DETERMINATION OF EFFECTIVE DEVICE PARAMETERS OF SILICON JUNCTION FIELD EFFECT TRANSISTORS

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DOCTOR OF PHILOSOPHY

By

PRASANTA KUMAR NANDI

to the

DEPARTMENT OF ELECTRICAL ENGINEERING

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CERTIFICATE

This is to certify that the research carried out by Prasanta Kumar Nandi for the preparation of the thesis 'DETERMINATION OF EFFECTIVE DEVICE PARAMETERS OF SILICON JUNCTION FIELD EFFECT TRANSISTORS' has been supervised by us. This thesis is being submitted to the Department of Electrical Engineering, Indian Institute of Technology, Kanpur, in partial fulfilment of the requirements for the degree of Doctor of Philosophy, and has not been submitted for a degree elsewhere.

Dr. R. Sharan
Professor,
Electrical Engg. Department
I.I.T. Kanpur.

Dr. R.N. Biswas
Professor,
Electrical Engg. Department
I.I.T. Kanpur.

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(P. K. Nandi)

CONTENTS

Page No.

Page No.

NOMENCLATURE

a	:	Total channel height
b_o	:	Residual channel height at the source
b_1	:	Residual channel height at the onset of velocity saturation
c_{ds}	:	Drain source small signal capacitance
c_g	:	Gate-channel capacitance
c_{iss}	:	Common source input capacitance
c_{gs}	:	Gate-source small signal capacitance
d	:	Ordinary differential operator
D	:	Suffix for drain/Extension of depletion region beyond gate
D_n	:	Diffusion constant for electrons
D_p	:	Diffusion constant for holes
E	:	Electric field
E_o, E_c	:	Critical electric field for velocity saturation
E_x	:	Electric field along the channel
F	:	Function of variables
G_n	:	Rate of generation of electrons
G_p	:	Rate of generation of holes
g_o	:	Open-channel conductance

g_{do} : Parallel channel conductance

g_{ds} : Incremental drain conductance

g_m : Mutual conductance

h : Depletion layer height in gradual channel

h' : Gate-channel depletion layer height

h'' : Substrate-channel depletion layer height

I_{CR} : Reverse saturation collector current

I_D : D. C. drain current

I_{ER} : Reverse saturation emitter current

I_G : Gate current

I_S : Maximum current in an undepleted channel/ Substrate current

i_D : Total instantaneous drain current

$\vec{J}$: Total current density

$\vec{J_n}$: Electron current density

$\vec{J_p}$: Hole current density

k : Dimensionless constant implying degree of velocity saturation / Boltzmann's constant

L : Length of the channel

n : Exponent/Electron density

N_o : Impurity concentration

N_{ref} : Reference impurity concentration for mobility calculation

p : Hole density

q : Electronic charge

r_{ds} : Incremental drain resistance

t : Time

u, u_1, u_2 : Non-dimensional residual channel heights

V_{bi} : Built-in voltage across P-N Junction

V_{DG} : Drain gate applied d-c bias

V_{Dp} : Drain voltage in excess of pinchoff

V_{DS} : Drain source applied d-c bias

V_{GD} : Gate drain applied d-c bias

V_{GS} : Gate source applied d-c bias

v_{DS} : Total instantaneous drain source bias

v_{GS} : Total instantaneous gate source bias

V_p : Pinchoff voltage

V_{pi} : Total reverse bias across gate and channel junction at pinchoff

v_s : Saturation drift velocity of carriers

$\vec{v}_n$: Drift velocity of electrons

$\vec{v}_p$: Drift velocity of holes

w	:	Normalised depletion layer width at source
w_{gc}	:	Gate channel depletion width
w_{sc}	:	Substrate channel depletion width
x	:	Length along the channel from source
x_1	:	Length of the gradual channel region
y	:	Depletion width in gradual channel
y_1	:	Total depletion width at source
y_2	:	Total depletion width at drain
z	:	Width of the channel
α	:	Exponent in Caughey-Thomas relationship
α_F	:	Forward current transfer ratio of parasitic junction transistor
α_R	:	Reverse current transfer ratio of parasitic junction transistor
α_{FD}	:	Value of α_F at drain
α_{FP}	:	Value of α_F at pinchoff in parallel channel
α_{FS}	:	Value of α_F at the source
δ	:	Partial differential operator
$\vec{\nabla}$	:	Vector differential operator
ε	:	Dielectric constant
η	:	Ideality factor

μ_o : Low field mobility

μ_{max} : Maximum mobility dependent on doping

μ_{min} : Minimum mobility dependent on doping

ρ : Charge density

σ_o : Low field conductivity

T : Temperature

LIST OF FIGURES

Page No.

Page No.

LIST OF TABLES

SYNOPSIS

DETERMINATION OF EFFECTIVE DEVICE PARAMETERS OF SILICON JUNCTION FIELD EFFECT TRANSISTORS

by
PRASANTA KUMAR NANDI
Department of Electrical Engineering
Indian Institute of Technology, Kanpur
INDIA
August, 1981

Most of the circuit parameters of semiconductor devices under normal operating conditions can either be obtained by direct measurements or be calculated from the knowledge of the device parameters (geometrical and material) by using the relationships between the circuit parameters and the device parameters. The values of such parameters are published by the device manufacturers and are freely available to circuit designers, whereas the values of the device parameters are generally far less accessible. In fact, even if the design values of these parameters are furnished, there is a certain amount of uncertainty in the actual device parameters that result during the fabrication process. Hence if, for any extended application of a device, a circuit designer is in need of extrapolating the values of certain circuit parameters of interest, he is left with two options :

(1) to measure the relevant circuit parameters under actual conditions of operation,

(2) to infer the values of the device parameters from measurements done under normal operating conditions and to use this knowledge for calculating relevant circuit parameters under extended conditions of operations. The former option, though seemingly straightforward, may present considerable practical difficulties. The objective of this thesis is to establish a methodology for the second option, specifically for the JFET.

Before one can actually select the two sets of parameters viz. device and circuit parameters, one must exercise caution to ensure that the relationships linking the chosen parameters are not mutually contradictory. One such inbuilt anomaly, which seems to have gone unnoticed by earlier workers arises out of the expressions for the channel conductance g_{do} and the gate-channel capacitance c_g in the voltage-variable-resistance (VVR) region of operation. This anomaly becomes evident from the following considerations.

(i) Experimental measurements of c_g for different values of the gate-source bias V_{GS} give a linear plot of $\frac{1}{c_g^2}$ vs V_{GS}, indicating an abrupt P-N junction with uniform doping.

(ii) Experimental measurements of the conductance g_{do} of the residual channel left after the formation of the gate-channel

depletion layer show that g_{do} varies linearly with the applied gate-source bias.

(iii) If the gate channel junction is indeed an abrupt P-N junction with uniform doping, g_{do} should be proportional to the square root of the applied gate-source bias.

Clearly, the three observations made above are not consistent. A conjecture for resolving this anomaly has been proposed on the basis of a parasitic transistor formed with the gate, channel and substrate of the JFET as its emitter, base and collector respectively. The generation of carriers in the gate-channel as well as in the substrate-channel depletion layers is shown to be capable of causing the width of the residual channel to vary linearly with the applied gate-source bias.

Device parameters for a planar JFET consist of channel dimensions (length, width and height) and the impurity profile. In the case of most commercially available JFETs the doping is uniform and as such the impurity profile is given simply by the constant impurity concentration. One thus has to select a set of four circuit parameters whose values can be conveniently and accurately measured. These four values can then be used to set up four independent equations involving the four device parameters. The selection of these four circuit

parameters out of the various possible choices is carried out in the following manner.

(1) The first consideration is the reliability of the relationships between the chosen circuit parameters and the device parameters. One thus makes the first short-list consisting of those circuit parameters which are related to the device parameters by well-accepted and preferably explicit relationships.

(2) A priority list is now prepared out of the short-listed circuit parameters on the basis of the convenience and accuracy of the necessary measurements.

(3) The first four parameters in the priority list are used in actual evaluation of the device parameters while some of the remaining are used in providing cross-checks.

This sequence of steps represents a general approach to the evaluation of the device parameters of any device from measurements of its circuit parameters. In case of JFET, this procedure is considerably simplified because of the nature of its models in the different modes of operation.

The parallel-channel behaviour of JFET is well understood and reliable; explicit relationships exist for the following three circuit parameters characterising this mode of operation.

i) Open-channel conductance g_o

ii) Pinchoff voltage V_p

iii) Reverse-bias gate-channel capacitance c_g.

It has been observed that no other independent relationship is available from the circuit parameters in the gradual-channel model. The common source input capacitance c_{iss} leads to an expression with device parameters which has been utilised later as a cross check.

For the fourth parameter, which should be independent with respect to the previous three, post-pinchoff models have therefore to be considered for obtaining another independent relationship between the two sets of parameters. As no satisfactory post-pinchoff model is available for short-channel JFETs, the methodology is restricted to long-channel devices only. Thus, it becomes necessary that a method be developed to distinguish long-channel and short-channel JFETs. Such a method has been developed on the basis of a property of the I_D-V_{DS} characteristic pointed out by Wedlock [1].

After a brief review of the different existing post-pinchoff models of long-channel JFETs, the two models suggested by Grebene and Gandhi [2], and Lehovec and Miller [3] have been tested for their agreement with experimental results. Only the following two circuit parameters have been found to have explicit mathematical expressions in terms of the device parameters which are verified experimentally.

i) Drain-source incremental conductance g_{ds}

ii) Gate-source incremental capacitance c_{gs}.

Of these two g_{ds} has been selected from the standpoint of the relative ease and accuracy of its measurement under pulsed biasing condition.

The four device parameters are determined uniquely from the measurements of the four circuit parameters. The device parameters so obtained are the effective parameters in the sense that these are capable of predicting only the electrical characteristics of the device and are not necessarily the parameters for the manufacture or design of the device. The validity of these effective device parameters has been established by the following checks done with the auxilliary measurements.

i) The dependence of c_{iss} on V_{DS} and V_{GS} has been derived for an experimental determination of the quantity $\frac{zL}{a}$ where z = channel width; L = channel length and a = undepleted channel height. The device parameters have been directly substituted to obtain this quantity which agrees within reasonable limits with the measured one.

ii) The dependence of c_{gs} on I_D and V_{GS} has been developed and the model has been tested for its validity through experimental measurements. A combination of the device parameters, $N_o^2 q^2 \mu_o a^2 z^2$ is directly obtained from the experimental measurements of this capacitance for different values of the bias currents and voltages. The value of this combination is obtained by a direct substitution of the

device parameters and is compared with the one obtained from the measurement of gate-source capacitance under post-pinchoff. The agreement within order of magnitude has been obtained indicating a fair validity of the model and the device parameters for long-channel commercially-packaged silicon JFETs.

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CHAPTER 1 : INTRODUCTION

The characteristics of semiconductor devices are analysed with the help of well-established physical laws of current transport, potential distribution and carrier continuity. The usual objectives behind such analysis are two fold :

i) to provide the device designer with the necessary functional relationships for meeting specific application requirements and

ii) to provide a model of the device to the application engineer for designing circuits using the device.

While the former objective is fulfilled by the manufacturing houses themselves through appropriate modifications and extensions of the established theory, the latter objective requires the manufacturer to visualise adequately the possible applications of the device. However, an ingenious circuit designer always finds some new interesting applications of the existing semiconductor devices beyond the domain of the applications visualised by the manufacturer. Such innovative ventures are often hindered by the absence of the right kind of data regarding the concerned device. This difficulty arises out of the limitations imposed by any model on the characterisation of the device. It would indeed be desirable to establish a methodology by means of which a circuit designer

is capable of obtaining a complete information on the device parameters (geometrical and material) through a few simple but accurate measurements on the device which effectively control the terminal characteristics he is interested in. Such a methodology, would, in general entail the following three distinct steps.

i) Representation of the device:inter-relationships among circuit properties and device parameters are obtained in the form of models by invoking the relevant physical laws.

ii) Determination of Device Parameters : the device parameters are estimated from experimental data on the circuit parameters, keeping in view the sensitivities of the measurements to the device parameters as well as to the environments.

iii) Validation of results : the model as well as the inferred values of the device parameters are cross-checked for consistency.

The junction field effect transistor (JFET) is a device where this problem is of particular significance due to the diverse range of its applications. The objective of the present investigation is to develop this methodology for JFET, so that, by using presently available information on the inter-dependence among its circuit parameters, it is possible to determine the values of the device parameters, which may then be utilised for

finding the parameters of any model.

It should be noted at this point that the values of the device parameters obtained through this exercise are 'effective' values, which need not be identical with the actual 'fabrication' parameters used by the manufacturer for the fabrication of the device. The implication of this deviation is crucial for the objective outlined earlier. While the fabrication parameters do form a basis for predicting the circuit properties of the device, it is well known that the final values of the parameters obtained after actual fabrication of the device do differ from the desired values. On the other hand, the 'effective' parameters obtained through the methodology adopted in this dissertation are based on circuit parameters themselves, and are as such more appropriate for assessing the performance of the device in usual as well as extended applications. In fact, the validation step is also to be interpreted in this light, the primary emphasis being on the consistency among the measured and predicted parameters.

1.1. Device parameters of a JFET

A simplified schematic diagram of an n-channel JFET is shown in Figure 1.1 where the terminal voltages and currents are indicated by their usual symbols. In principle, a circuit model for the device may be obtained

to suit any application at hand provided the functional dependences of the currents i_D and i_G on the voltages v_{DS} and v_{GS} are explicitly known. These functional dependences can be determined, in principle, through a solution of the mobile-charge continuity, Poisson and current transport equations (written below for semiconductor devices in general) subject to the boundary conditions imposed by the applied voltages v_{DS} and v_{GS} :

$$\frac{\delta n}{\delta t} = G_n - U_n + \frac{1}{q} \vec{\nabla} \cdot \vec{J_n} \qquad .. \quad (1.1)$$

$$\frac{\delta p}{\delta t} = G_p - U_p - \frac{1}{q} \vec{\nabla} \cdot \vec{J_p} \qquad .. \quad (1.2)$$

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon} \qquad .. \quad (1.3)$$

$$\vec{J_n} = q D_n \vec{\nabla} n + q n \vec{v_n} \qquad .. \quad (1.4)$$

$$\vec{J_p} = -q D_p \vec{\nabla} p + q p \vec{v_p} \qquad .. \quad (1.5)$$

$$\vec{J} = \vec{J_n} + \vec{J_p} + \varepsilon \frac{\delta \vec{E}}{\delta t} \qquad .. \quad (1.6)$$

Here the symbols have their usual meaning. For n-channel JFET these equations become simplified, due to the absence of generation and recombination and the predominance of drift in the conduction current as follows :

$$\frac{\delta n}{\delta t} = \frac{1}{q} \vec{\nabla} \cdot \vec{J} \qquad .. \quad (1.7)$$

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon} \qquad .. \quad (1.8)$$

$$\vec{J} = qn\vec{v_n} + \varepsilon \frac{\delta \vec{E}}{\delta t} \qquad .. \quad (1.9)$$

The mechanisms that lead to the conduction component of the gate current have been ignored here because this component has a very small magnitude under normal operating conditions.

In order to obtain the drain current i_D and the displacement component of the gate current i_G from the solution of the equations (1.7) to (1.9), a knowledge of the values of the following parameters is necessary :

i) the height of the undepleted channel 'a',

ii) the length of the channel 'L',

iii) the width of the channel 'z',

iv) the distribution of the charge density 'ρ',

v) the carrier density in the channel 'n',

vi) the velocity-field characteristic in the channel (i.e. saturated velocity 'v_s' and mobility 'μ_o')and

vii) the dielectric constant of the semiconductor 'ε'.

The channel dimensions a, z, L (indicated in Figure 1.1) constitute the geometrical parameters of the device. Of the material parameters constituting the remaining data needed for the solution of the equations, dielectric constant and saturation velocity of the

majority carriers are intrinsic properties of the semiconductor, while ρ and n both depend on the profile of the impurity concentration N_o. One more parameter of interest, which is also affected by the manufacturing process is the drift mobility μ_o which determines the dependence of carrier velocity on the electric field in the linear region of the velocity-field characteristic. The following empirical expression for μ_o in terms of N_o has been given by Caughey and Thomas [1]*.

$$\mu_o = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_o}{N_{ref}}\right)^{\alpha}} \qquad .. \quad (1.10)$$

Thus the complete set of 'device parameters' consists of the geometrical parameters a, z and L and the material parameters N_o and μ_o, if the Caughey-Thomas relationship is not exploited. However, by using this interdependence of N_o and μ_o the number of device parameters can be reduced to four (a, z, L, N_o).

1.2. Circuit parameters of JFET

Any attempt to correlate the device parameters to a chosen set of circuit parameters has to be based on well-established analytical or empirical relationships. While looking for such relationships one must exercise

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* Numbers in brackets designate References at the end of each Chapter.

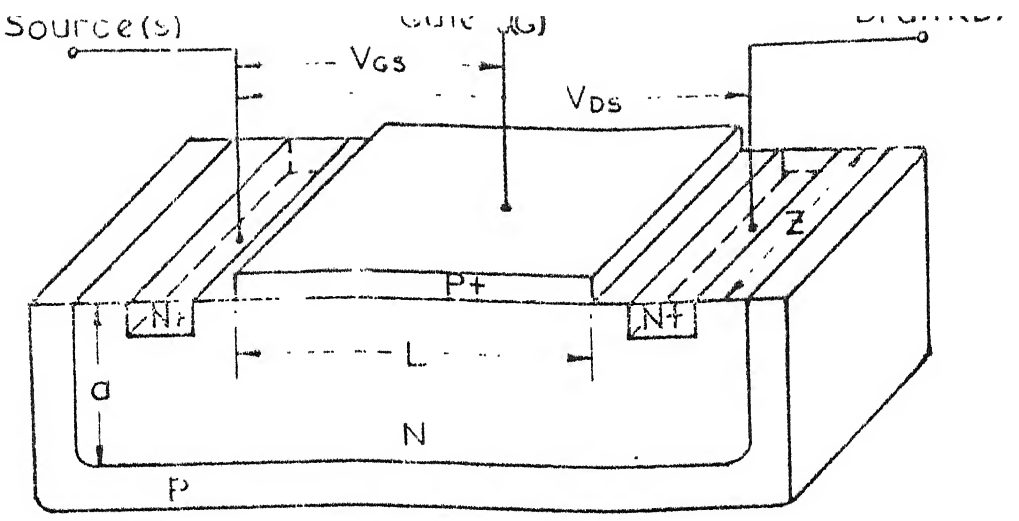
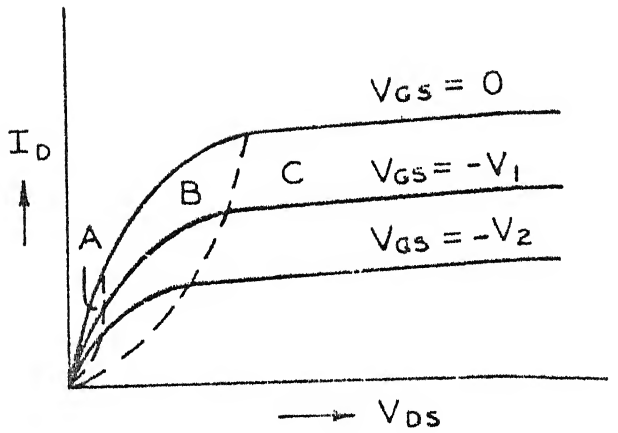


FIGURE 1.1 GEOMETRICAL CONFIGURATION OF A PLANAR N-CHANNEL JFET.



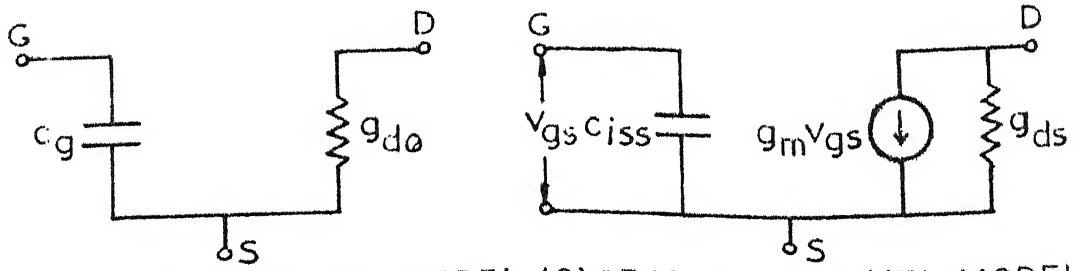
$0 < |V_1| < |V_2|$

Region A – Parallel channel

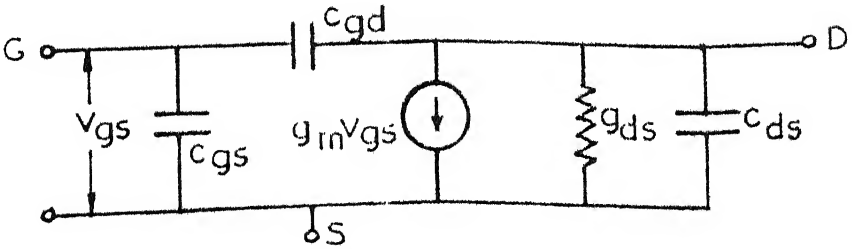
Region B – Gradual channel

Region C – Post-pinch off

(a) $i_D - V_{DS}$ CHARACTERISTICS (n-CHANNEL)



) PARALLEL-CHANNEL MODEL (C) GRADUAL-CHANNEL MODEL



(d) POST-PINCH OFF MODEL

RE 1.2 THE THREE REGIONS OF OPERATION OF A JFET

a lot of caution as even analytical approaches based on well-founded theories may lead to results not corroborated by experiments. An interesting example of such an anomaly has been found in the course of this work and is discussed in the next chapter.

As the present objective can be served only by proven relationships among the device and circuit parameters, it is absolutely essential to confine our attention to the set of independent circuit parameters from those widely used in practical applications.

1.2.1. Circuit parameters and the physical models

The geometrical configuration of a planar JFET is shown in Figure 1.1 with a donor doped channel. The substrate and the gate are doped with acceptor impurities; the gate is heavily doped while the substrate doping is somewhat lighter than that of the channel.

This structure of JFET has been commonly used for modelling by many workers. In the following subsections a classification of the models based on the applied bias voltages has been discussed. Also the different circuit parameters which have been evolved from each class of physical models are also put forward in a table for a closer examination of the relative ease and accuracy of their measurements.

Physical modelling of JFET has been pioneered by Shockley with his gradual channel approximation. The gradual-channel model as conceived by Shockley does not contribute much towards the evolution of the circuit parameters of JFET and can not be used for analysis of circuits; yet it is the most important physical model from the point of view of basic understanding of the physical phenomena in JFETs.

The other classes of physical models are, on the other hand based on circuit applications. The principal use of JFET lies in the input stage of voltage amplifiers because of the inherent high impedance and low-noise capability of the device. The physical model developed for this circuit application of JFETs is the post-pinchoff model where the phenomenon of current saturation in the channel aids to its application as an amplifier. Another important area of application of JFET exploits its voltage-variable resistance (VVR) property at low values of drain-source voltage v_{DS}. A special case of VVR operation is the low level sampling gate which is perhaps as important an application of JFET as any other. The relevant physical model is the parallel-channel model. The different regions of operation of JFETs, along with the corresponding small-signal equivalent circuits, are shown in Figure 1.2. The resulting classification of the physical models representing

these different regions as well as the relevant circuit parameters is given in table 1.1. The expressions relating the parameters defined in table 1.1 to the device parameters are examined in chapters 2, 3 and 4 for their acceptability.

Table 1.1 JFET Circuit parameters

Region	Model	Bias Voltages			Circuit parameters	
		$\left\|\frac{V_{DS}}{V_p}\right\|$	$\left\|\frac{V_{GS}}{V_p}\right\|$	$\left\|\frac{V_{DG}}{V_p}\right\|$	Static	Dynamic
A	Parallel-Channel	$\ll 1$	<1	<1	$g_{do}=\frac{\delta i_D}{\delta v_{DS}}$	c_g (gate-channel capacitance)
B	Gradual-channel	<1	<1	<1	$g_m=\frac{\delta i_D}{\delta v_{GS}}$ $g_{ds}=\frac{\delta i_D}{\delta v_{DS}}$	c_{iss} (common source input capacitance)
C	Post-pinchoff	>1	<1	>1	$g_{ds}=\frac{\delta i_D}{\delta v_{DS}}$ $g_m=\frac{\delta i_D}{\delta v_{GS}}$	c_{gs} (gate source cap.) c_{gd} (gate drain cap.) c_{ds} (drain source cap.)

1.3. Formulation of the problem

The purpose of the present work is to obtain the values of the device parameters of a JFET from the knowledge of the values of a selected set of circuit parameters. As the number of circuit parameters available from various models would considerably exceed the number of device parameters, the procedure for selecting the set of circuit parameters to be used involves the following steps :

i) Identification of a set of circuit parameters related to the device parameters through well-established physical or empirical relationships.

ii) Determination of the device parameters from a minimal set of circuit parameters chosen out of the possible 'adequate' sets which are sufficient for obtaining a unique solution.

iii) Calculation of other circuit parameters from the values of device parameters already obtained, and cross-checking them with experimental data.

These steps constitute the methodology given at the beginning of this chapter and are developed and carried out in chapter 5. The relationships actually utilised for the purpose are developed through studies of available models of JFETs starting with the parallel-channel model in chapter 2, gradual-channel and post-pinchoff models in chapters 3 and 4 respectively.

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CHAPTER - II

PARALLEL CHANNEL MODEL AND DEVICE PARAMETERS

The parallel channel model of JFET applies to the situation where the magnitude of the drain-source voltage v_{DS} is negligible in comparison with the pinch off voltage v_p, so that the depletion layer remains essentially parallel to the gate-channel boundary. Before exploiting the existing physical models for this region of operation, the possible effects of a hitherto neglected aspect of planar JFET, viz. the floating substrate are considered. In the following sections the effect of the substrate on the models for this region of JFET operation is investigated and is shown to be capable of explaining observed discrepancies between some existing models and experimental data.

2.1. Effect of substrate

It is evident from Figure 1.1 that the substrate terminal is not connected to any external lead of the device. Thus, there is no current in the substrate and hence its effect has to be purely electrostatic. The depletion layer in the channel region due to substrate-channel junction is the only mechanism which might affect the terminal characteristics of JFETs. This depletion

layer may either have a constant width independent of bias voltages applied to the device, or may vary with the applied bias voltages. In the former case, the existence of the substrate would lead to a fixed change in the effective channel height 'a', thus resulting in quantitative changes in the model parameters (e.g. in the value of the pinch off voltage). In the latter case the dependence of the terminal currents on the applied voltages would undergo a qualitative change. It is, therefore, of interest to examine how the substrate-channel depletion is affected by the applied bias voltages.

2.1.1. Parasitic elements in JFET

A convenient way of analysing the possible contributions of the substrate is to consider a parasitic element involving the substrate and other active regions of the device. A perusal of the planar configuration of an n-channel JFET shown in Figure 1.1 reveals the presence of a vertical PNP transistor. The noteworthy features of this particular parasitic element are the following :

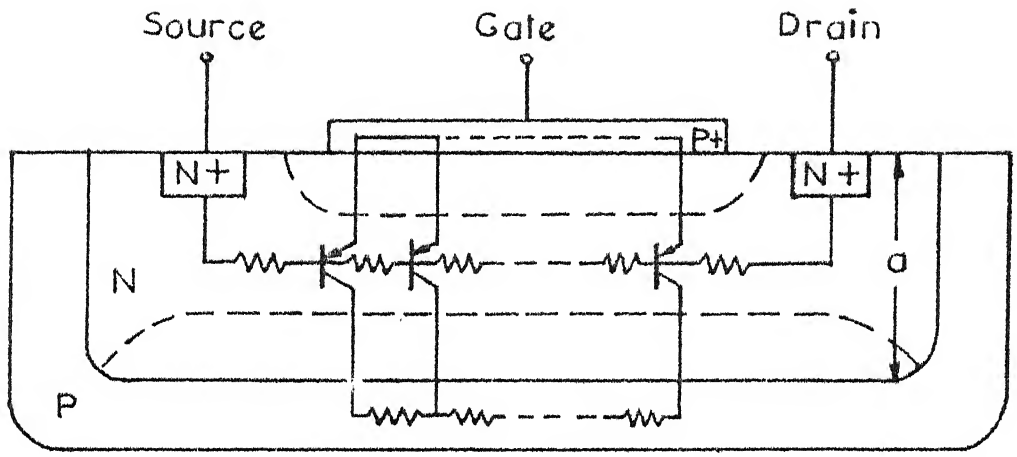
1) the emitter of the transistor is the gate of the JFET which is degenerately doped,

2) the base region is the part of the channel directly under the gate having a width of 1 to 5 μM with a moderate doping, and

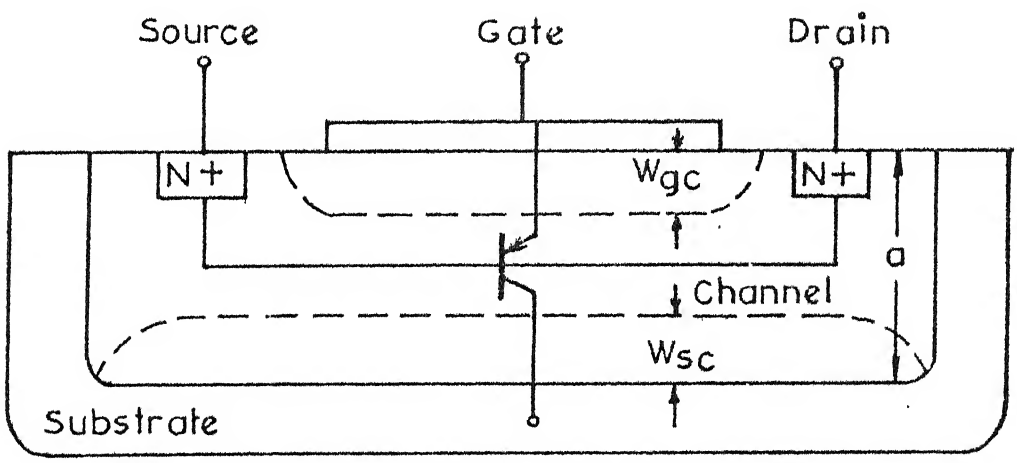
3) the collector region is the substrate which has the largest area in comparison with the areas of emitter and base.

This parasitic PNP transistor would have a reasonable forward current gain due to the fact that the structure and the doping levels in different regions are more or less compatible with the ones fabricated conventionally. The transistor in this form is indeed fabricated deliberately while integrating a n-channel JFET and a PNP transistor on the same chip. Lin [1] has considered the parasitic JFET action in such vertical PNP transistors. It will not be out of place to add that such vertical transistors with JFET devices from the super-alpha combination - a popular composite device used in the area of analog circuit design for buffers and voltage followers. In all these cases, however, the parasitic PNP transistor action within the channel of the JFET has not been taken into consideration.

For the present analysis a distributed model of the parasitic PNP transistor is considered as shown in Figure 2.1(a). The emitters of all the parasitic PNP transistors are connected to the gate, which has negligible resistivity. The conductivity of the channel is modulated by the applied electrical biases to the JFET



(a) JFET STRUCTURE WITH DISTRIBUTED PARASITIC ELEMENT



(b) JFET STRUCTURE WITH LUMPED PARASITIC FOR PARALLEL-CHANNEL OPERATION

FIGURE 2.1 JEFT STRUCTURE SHOWING THE PARASITIC ELEMENT

terminals. Hence the bases of all the parasitic transistors are connected by a chain of resistances terminating into the drain and source contacts. The substrate does not carry any current. Therefore, the collectors of all the parasitic transistors are at the same potential.

A further simplification of the parasitic transistor structure is possible for the parallel-channel operation. As the voltage drop along the channel is negligible in this region, the bases of the distributed transistors can be considered to be at the same potential. Accordingly, the distributed transistor structure shown in Figure 2.1(a) may now be lumped into a single transistor as shown in Figure 2.1(b) which also shows the connections of the relevant terminals of the transistor with those of the JFET.

2.2. Analysis of the parasitic transistor

It is evident from the biasing of JFET in the parallel-channel region that the collector-base and the emitter-base junctions of the equivalent parasitic PNP transistor shown in Figure 2.1(b) are both reverse biased. For obtaining the voltage-current relationships of the parasitic transistor under this biasing condition the model proposed by Ebers and Moll [2] is employed which is capable of analysing the cut-off mode behaviour of bipolar junction transistors, a situation identical with the

present one. At the same time, it is also well-known that Ebers-Moll model is proposed to explain the injection currents and their voltage dependences. As this model explains the behaviour of junction transistors under cut-off mode also, the model seems to be adaptable for transistors where not only injection is the mechanism of current conduction but also other mechanisms like generation and recombination are prevalent:with this concept in view, one proceeds to determine the relationships between the voltages and the currents of the parasitic PNP transistor.

The principal mechanism responsible for conduction of current under reverse bias or very small forward bias is the generation of excess carriers in the depletion region. Diffusion of minority carriers leading to carrier injection is rather insignificant under such circumstances. This is corroborated by the experimental current-voltage relationship of Silicon diodes at room temperature under reverse bias, satisfying the equation

$$I = I_o \left[\exp \left(\frac{qv}{\eta kT} \right) - 1 \right] \qquad .. \quad (2.1)$$

instead of

$$I = I_o \left[\exp \left(\frac{qv}{kT} \right) - 1 \right] \qquad .. \quad (2.2)$$

where the latter is obtained in the case where the ideality factor $\eta = 1$, from equation (2.1). The assumption of a pure diffusion phenomena leads to equation (2.2).

The application of Ebers-Moll equations to the parasitic transistor in Figure 2.1(b) yields

$$I_G = I_E = I_{ER} - \alpha_R I_{CR} \quad .. \quad (2.3)$$

where I_{ER} and I_{CR} are the reverse bias saturation currents for the emitter-base and collector-base junctions respectively and α_R is the reverse current transfer ratio. I_G is the gate current of the JFET.

The floating substrate of the JFET results in zero collector current for the parasitic transistor. So,

$$I_S = I_C = 0 = I_{CR} - \alpha_F I_{ER} \quad .. \quad (2.4)$$

where α_F is forward current transfer ratio of the parasitic transistor. From equations (2.3) and (2.4), it is straight forward to obtain

$$I_{ER} = \frac{I_G}{1 - \alpha_R \alpha_F} \quad .. \quad (2.5)$$

and

$$I_{CR} = \frac{\alpha_F I_G}{1 - \alpha_R \alpha_F} \quad .. \quad (2.6)$$

At this point, it is essential to have a knowledge of the mechanism of conduction of these currents through the parasitic transistor so that their dependence on the depletion layer widths w_{sc} and w_{gc} and on the applied bias V_{GS} may be formulated.

The present investigation being solely confined

to Silicon JFETs, the reverse bias currents have been assumed to depend mostly on the generation of excess carriers in the depletion layers. The validation of this assumption by an indirect experiment is discussed afterwards.

The model suggested by Sah, Noyce and Shockley [3] for generation-dominant characteristics of semiconductor devices is therefore used to obtain a direct relationship between the current I_{ER}, I_{CR} and the depletion layer widths w_{gc}, w_{sc} as follows :

$$I_{ER} \propto w_{gc} \qquad .. \quad (2.7)$$

$$I_{CR} \propto w_{sc} \qquad .. \quad (2.8)$$

wherefrom

$$\frac{w_{sc}}{w_{gc}} = \frac{I_{CR}}{I_{ER}} = \alpha_F \qquad .. \quad (2.9)$$

Here α_F is the common base short circuit current gain of the parasitic PNP transistor. Equation (2.9), therefore, leads to the conclusion that the substrate-channel depletion layer width w_{sc} and gate-channel depletion layer width w_{gc} are not independent with respect to each other. The gate-channel depletion layer width w_{gc} being adjustable with externally applied bias, it may be concluded that the substrate-channel depletion layer width w_{sc} also changes in the same way as that of the gate-channel junction.

In the context of this discussion, it may be added

that the analysis of the JFET in the parallel-channel region is of direct relevance in explaining the operation of the device as a low level switch. A single depletion layer has been conceived earlier for the model of parallel-channel operation of the device. Now, with the incorporation of the effects of the substrate, the active channel height available for conduction has to be considered with a two-fold dependence on the gate-channel bias and is presented in the following section.

2.3. Parallel-channel model incorporating the effect of the parasitic transistor

As mentioned in table 1.1 the following two parameters are relevant for the parallel-channel model :

i) gate-channel capacitance c_g, and

ii) channel conductance g_{do}.

Both these parameters are dependent on the applied bias V_{GS} which should be in the range $0 < V_{GS} < V_p$ for p-channel devices and $-V_p < V_{GS} < 0$ for n-channel devices. These two parameters are given in terms of the device parameters and the depletion layer widths w_{gc} and w_{sc} as follows :

$$c_g = \frac{\varepsilon z L}{w_{gc}} \qquad .. \quad (2.10)$$

and

$$g_{do} = g_o \left(1 - \frac{w_{gc} + w_{sc}}{a} \right) \qquad .. \quad (2.11)$$

where $$g_o = \frac{N_o q \mu_o az}{L} \qquad .. \quad (2.12)$$

is the conductance of the undepleted channel, assumed to be homogeneously doped with a constant impurity concentration. The gate-channel depletion width w_{gc} may be expressed for a one-sided abrupt junction with uniform doping as

$$w_{gc} = \sqrt{\frac{2\varepsilon\ (|V_{GS}| + V_{bi})}{N_o\ q}} \qquad .. \quad (2.13)$$

If one puts

$$V_{pi} = \frac{N_o\ q\ a^2}{2\varepsilon}, \qquad .. \quad (2.14)$$

w_{gc} may be expressed as

$$w_{gc} = a \sqrt{(|V_{GS}| + V_{bi})/V_{pi}} \qquad .. \quad (2.15)$$

The physical significance of V_{pi} will be brought out later. Using equations (2.9) and (2.14), equation (2.11) can be rewritten as

$$g_{do} = g_o \left[1 - (1+\alpha_F) \sqrt{\frac{|V_{GS}| + V_{bi}}{V_{pi}}}\ \right]: \ |V_{GS}| \leqq V_p \qquad .. \quad (2.16)$$

An expression for the pinchoff voltage V_p can now be obtained by setting $g_{do} = 0$ for $V_{GS} = V_p$ in equation (2.16).

$$V_p = \frac{V_{pi}}{(1+\alpha_F)^2} - V_{bi} \qquad .. \quad (2.17)$$

If the effect of the substrate is neglected i.e. one assumes $\alpha_F = 0$, equations (2.16) and (2.17) reduce to

$$g_{do} = g_o \left[1 - \sqrt{\frac{|V_{GS}| + V_{bi}}{V_{pi}}} \right] \qquad .. \quad (2.18)$$

and $$V_p = V_{pi} - V_{bi} \qquad .. \quad (2.19)$$

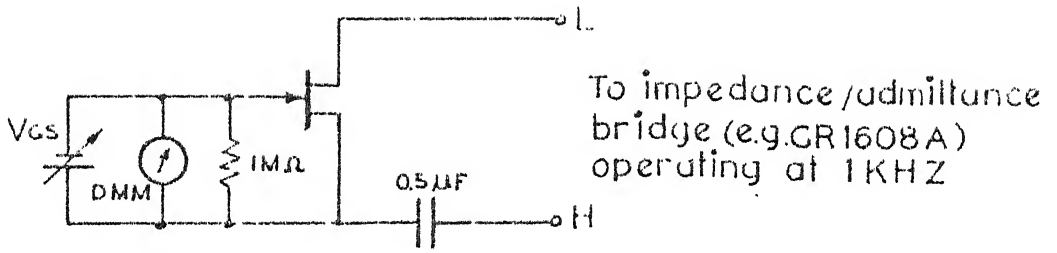
Thus, V_{pi} is simply the total reverse bias on the gate-channel junction (including the built-in voltage V_{bi}) required for pinchoff if the effect of the substrate is not considered. Equation (2.18) is the usual relationship given in the literature [4] for g_{do} as a function of V_{GS}. It is interesting to note that the expression for c_g as given in equation (2.10) is independent of α_F and, as such, irrespective of whether the effect of the substrate is considered or not, one has the equation relating c_g with V_{GS} as

$$c_g = \frac{\varepsilon z L}{a} \sqrt{\frac{V_{pi}}{|V_{GS}| + V_{bi}}} \qquad .. \quad (2.20)$$

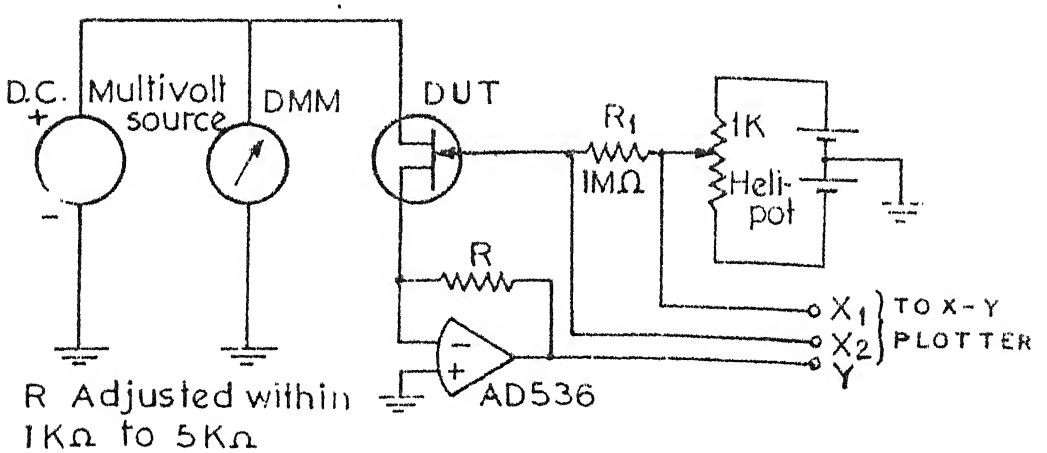
In order to decide about the validity of the models for g_{do} and c_g, experiments are carried out to observe the dependences of g_{do} and c_g on V_{GS}.

2.3.1. Experimental techniques for the measurement of g_{do} and c_g

Figure 2.2(a) shows the schematic for the conventional method of the measurement of g_{do} using an admittance bridge. One has to be careful that the magnitude of the a-c drain-source voltage is kept small in comparison with the d-c bias throughout the measurement. A novel



(a) CONVENTIONAL METHOD OF MEASUREMENT OF CHANNEL CONDUCTANCE



b METHOD OF MEASUREMENT OF g_o & V_{bi}

FIGURE 2.2 METHOD OF MEASUREMENT OF g_{do} VS V_{GS} CHARACTERISTICS

scheme of measurement has been developed in the course of the present work which measures not only g_{do} as a function of V_{GS} but also provides the facility to obtain the value of the built-in voltage V_{bi}, which is a parameter otherwise difficult to measure. Besides, with a little modification of this scheme of measurement it is also possible to obtain a continuous plot of the open channel conductance g_o against temperature over a wide range. The set up is shown in Figure 2.2(b) and is described as follows.

A small d-c voltage (of the order of 50 mv) is applied between drain and source and the current flowing through the channel is converted into a voltage with the help of an opamp. This voltage is fed to the Y input of an X-Y plotter for a continuous recording. The gate-source bias V_{GS} is derived from a low resistance helical potentiometer (1 k ohm) for the provision of a smooth and continuous variation of the bias. The output from the potentiometer is connected to the gate of the device under test through a high series resistance R_1 (1 M ohm), so that in the event of a forward bias, the voltage drop across the resistance would indicate the flow of gate current. The points marked as X_1 and X_2 are alternately connected to the X input of the recorder for two successive plots obtained with the variation of V_{GS}.

A typical experimental plot of g_{do} vs V_{GS} for an n-channel device using this method, is shown in Figure 2.3(a). The following features of this plot are of interest.

i) The two plots coincide for $V_{GS} < V_A$, while they sharply diverge for $V_{GS} > V_A$, implying that in the region to the left of point A the current drawn by the gate causes a voltage drop across R_1 so that the voltages at points X_1 and X_2 are not the same.

ii) Point A thus marks the value of V_{GS} which just annuls the built-in potential V_{bi}. Hence, one directly obtains the value of V_{bi} ($= V_A$) from the plot.

iii) When the gate-channel junction is progressively reverse-biased a point B is reached where the drain current becomes zero. The magnitude of V_{GS} at this point gives the value of V_p.

iv) The value of the open-channel conductance g_o is directly given as the value of g_{do} at point A.

For the purpose of a continuous plot of g_o with temperature, the potentiometer is removed and a constant gate current of the order of 1 μA is applied. The purpose of this current is to bias the gate-channel junction just at the threshold of conduction i.e. at point A of Figure 2.3(a). The gate voltage developed at this point is the built-in voltage V_{bi} which is a measure of the temperature of the junction; it is well known that the built-in voltage

for a lightly doped abrupt silicon P-N junction changes at the rate of 2.2 mV/^{o}C over a wide range of temperature [5]. This gate voltage is therefore connected to the X input and a voltage proportional to the drain current is fed to the Y input to obtain a g_o vs temperature plot. A large thermal mass is attached to the header containing the device so as to ensure a slow rate of change of temperature. An experimentally obtained plot for g_o vs temperature is shown in Figure 2.3(b), along with an experimental plot for the low field mobility μ_o as a function of temperature [6]. The trend of the two curves are alike over a large range of temperature, leading to the conclusion that the product of N_o az/L remains fairly constant with respect to the temperature, as expected.

The characteristics of gate-channel capacitance c_g with reverse bias V_{GS} is obtained by the conventional method using a capacitance bridge. In this work, the capacitance bridge model Boonton-74C operating at 100 KHZ has been used. As equation (2.20) predicts a linear relationship between $(\frac{1}{c_g})^2$ and $|V_{GS}|$, the experimental data have been accordingly plotted in Figure 2.3(c).

2.3.2. An anomaly and a conjecture for resolving it

The experimentally observed variations of g_{do} and c_g with V_{GS} present a serious anomaly. As the plot of $(\frac{1}{c_g})^2$ vs V_{GS} is a straight line, equation (2.20)

is verified, justifying the previous assumption of an abrupt junction and a uniformly doped channel. If the effect of the substrate is indeed negligible, equation (2.18) should be satisfied, which predicts a parabolic relationship between g_{do} and V_{GS}; the experimental plot of g_{do} vs V_{GS}, on the contrary, is a straight line over most of the range of V_{GS}. Experiments on a large number of commercially available JFETs lead to the same anomaly.

It is felt that this anomaly is a consequence of the fact that the depletion layer at the substrate-channel junction has been left out of consideration in obtaining equation (2.18). It has been shown that a more general relationship between g_{do} and V_{GS} is given by equation (2.16), which is reproduced below for convenience.

$$g_{do} = g_o \left[1 - (1+\alpha_F) \sqrt{\frac{|V_{GS}| + V_{bi}}{V_{pi}}} \right] : |V_{GS}| \leq V_p \quad .. \quad (2.16)$$

It should be noted that if α_F is independent of V_{GS} this equation also gives a parabolic plot of g_{do} vs V_{GS} and the anomaly remains unresolved. It is our conjecture that, for a suitable functional dependence of α_F on V_{GS}, g_{do} can become a linear function of V_{GS}, at least over a substantial region.

Experiences with silicon transistors do show that α_F has a significant variation with bias voltages and the

phenomenon has contributed to the development of a very useful device viz. silicon controlled rectifier. The laws of variation of α_F with applied bias under the condition of both junctions in reverse bias has not been explored so far to the best of the information available.

Let the value of α_F at pinchoff be designated as α_{FP}. One notes that the value of α_F to be used in equation (2.17) is α_{FP} and thus obtains the expression

$$(1 + \alpha_{FP})^2 \ (V_p + V_{bi}) = V_{pi} \qquad .. \quad (2.21)$$

Equation (2.16) may now be rewritten as

$$g_{do} = g_o \left[1 - \frac{1 + \alpha_F}{1 + \alpha_{FP}} \sqrt{\frac{|V_{GS}| + V_{bi}}{V_p + V_{bi}}} \right] \qquad .. \quad (2.22)$$

The experimental data, on the other hand, may be expressed in terms of the empirical relationship

$$g_{do} = g_o \left[1 - \frac{|V_{GS}| + V_{bi}}{V_p + V_{bi}} \right] \qquad .. \quad (2.23)$$

One can compare equations (2.22) and (2.23) to obtain

$$\frac{1 + \alpha_F}{1 + \alpha_{FP}} = \sqrt{\frac{|V_{GS}| + V_{bi}}{V_p + V_{bi}}} \qquad .. \quad (2.24)$$

This requires α_F to be a montonically increasing function of the applied bias V_{GS}, the nature of the function being shown in Figure 2.4. That such a variation of α_F with V_{GS} is indeed plausible may be seen from a consideration of the mechanism of current transport in junction transistors.

The base transport factor is enhanced by the reduction of the base thickness in a bipolar junction transistor. This is also a cause for the increase in the forward current gain with increase in collector-base bias. As the depletion layers at the gate-channel and the substrate-channel junctions of a JFET widen due to the application of V_{GS}, the equivalent base width of the parasitic transistor (i.e. the residual channel width of the JFET) decreases resulting in an increase in α_F .

The effect of the parasitic transistor thus leads to a plausible explanation of the experimentally observed g_{do} vs V_{GS} variation as given by equation (2.23). The assumption forming the basis of this analysis is that the reverse bias currents depend mostly on the generation of excess carriers in the depletion layers as stated in section 2.2.2. It is therefore necessary to validate this assumption before one can use the parallel-channel model with confidence.

2.3.3. Experimental validation of the assumption

Let us start with the question whether an experiment can be designed to validate the assumption mentioned above. In this regard, the following facts in the mechanism of current transport in a P-N junction may be noted.

i) Depending upon the band gap of the semiconductor and the applied bias the current through a

P-N junction flows either due to recombination/generation in the depletion region or by the diffusion in the quasi-neutral region or by a mixture of the two, the two extreme cases corresponding to the value of the ideality factor $\eta=2$ and $\eta=1$ respectively.

ii) the current which is controlled by generation/recombination is proportional to the intrinsic carrier concentration n_i whereas that controlled by diffusion is proportional to n_i^2. As a result, the latter component increases faster with rise in temperature than the former leading to a diffusion dominant current at 'high' temperatures whereas the recombination/generation component is dominant at 'low' temperatures (provided the current-either forward or reverse is low).

iii) the temperature discriminating the dominance of one or the other mechanism depends on the band gap of the material.

It is due to these facts, that one finds the value of the ideality factor $\eta = 1$ for the entire forward bias region in Germanium P-N junctions at room temperature whereas at liquid nitrogen temperatures the same P-N junction shows the value of $\eta = 2$ at low forward bias. For P-N junction in silicon which has a larger band gap even at room temperature one finds the dominance of generation currents at low forward bias leading to $\eta = 2$.

However, at sufficiently high temperatures the diffusion becomes the dominant mechanism of current conduction even in silicon. Therefore, to test the validity of the assumptions mentioned above, the g_{do} vs V_{GS} characteristics is measured both at room temperature and at a substantially high temperature. The resulting plots shown in Figure 2.4 indicates a linear relationship at room temperature but a trend towards a parabolic relationship at high temperature indicating that the device tends to satisfy equation (2.18) obtained by neglecting the effect of the substrate at high temperature. It is thus established that the linear characteristic of g_{do} vs V_{GS} of silicon devices as observed experimentally is indeed a consequence of the interaction of the two depletion layers through the generation/recombination based Sah-Noyce-Shockley model.

2.4. Device parameter relationships available from parallel channel model

The plot of $\left(\frac{1}{c_g}\right)^2$ vs V_{GS} yields a combination of the device parameters as its slope. As pointed out earlier, this relationship is quite reliable and can be used with confidence for evaluating the device parameters.

The nature of variation of g_{do} with V_{GS} on the other hand can not be utilised due to the uncertainty in the mechanism of current transport as well as in the value of α_F. Only the values of g_o and V_p can therefore be used for the purpose of the present problem.

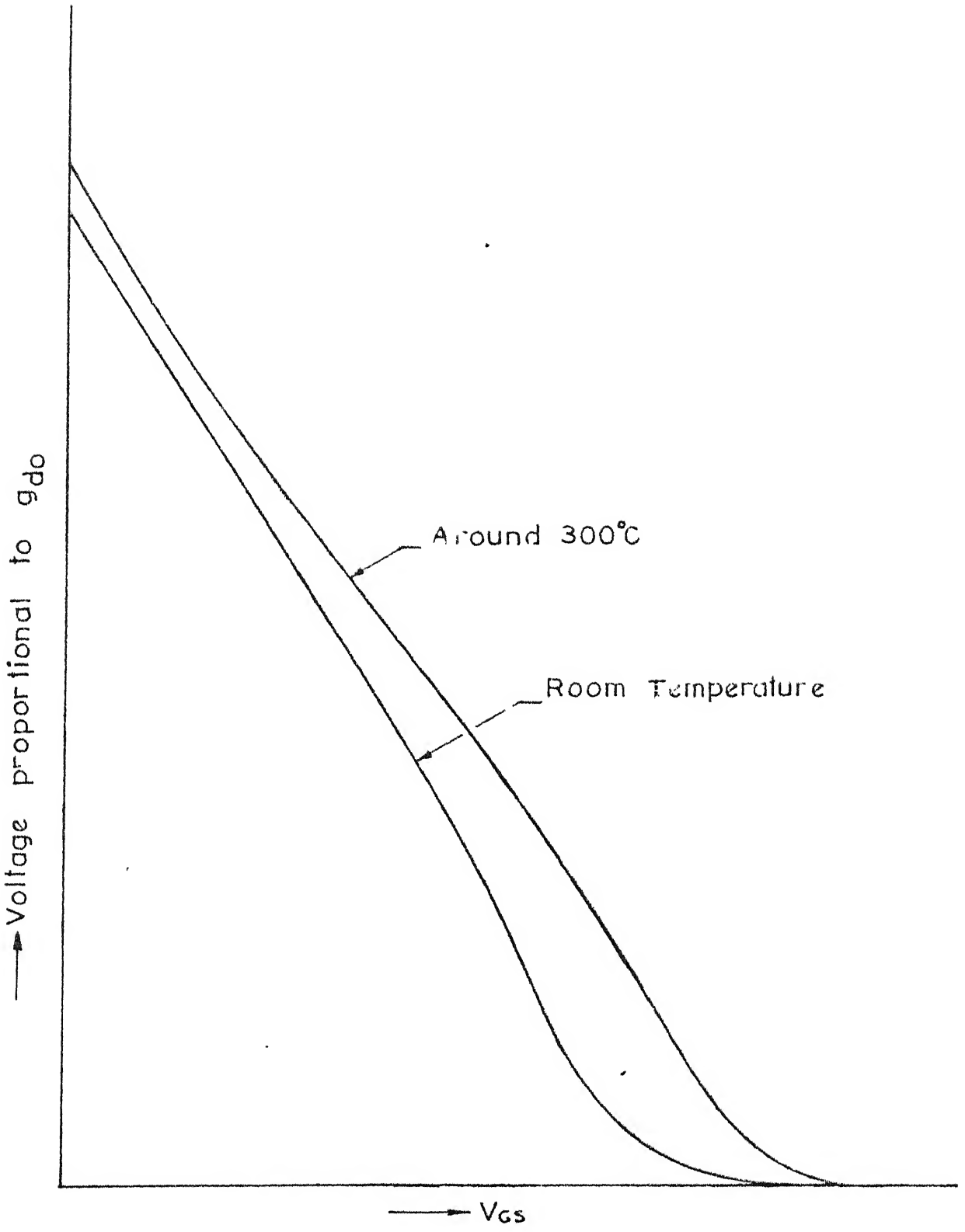


FIGURE 2.4 PLOT OF g_{do} Vs. V_{GS} AT ROOM TEMPERATURE

It is thus concluded that the parallel-channel model may be utilised to obtain the following three device parameter relationships.

i) $$\frac{N_o q \mu_o a z}{L} = g_o$$

ii) $$\frac{N_o q a^2}{2\varepsilon} = V_p + V_{bi}$$

iii) $$\frac{2}{\varepsilon N_o q (zL)^2} = \frac{d\left(\frac{1}{C_g}\right)^2}{d(-V_{GS})}$$

The actual procedure for utilising these data along with the informations available from other models will be taken up in Chapter 5.

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CHAPTER - III

GRADUAL CHANNEL MODEL

The gradual-channel model applies for the range of operation where the applied bias voltage V_{GD} between gate and drain does not exceed the pinchoff voltage V_p. In this mode of operation the variation of the depletion layer from source to drain is assumed to be gradual and current continuity in the channel is maintained through an appropriate variation of the drift velocity of carriers along the channel, the maximum carrier velocity within the channel being less than the saturation velocity. This assumption referred to as the gradual channel approximation, is due to Shockley [1] and is valid only for long-channel JFETs which have the ratio of length 'L' to the height 'a' of the channel large compared to unity. This simplifying step enables one to decompose the inherently two-dimensional continuity and Poisson equation into two one-dimensional problems, thereby permitting closed-form mathematical solutions.

The following terminal characteristics are relevant to the gradual-channel model.

i) Channel current I_D as a function of V_{GS} and V_{GD}.

ii) Input capacitance C_{iss} under common source configuration as a function of V_{GS} and V_{GD}.

3.1. JFET characteristics in gradual channel region

Figure 3.1(a) shows the depletion regions in the gradual-channel operation of JFET. The parasitic transistors arising out of the effects of substrate is shown in Figure 3.1(b). The drain-characteristics of the device has been obtained both for constant mobility and field dependent mobility of the carriers in the channel. The present analysis has been carried out on the basis of constant mobility.

3.1.1. Analysis of gradual-channel region with constant mobility

Following the method of Bockemuehl [2] for a homogeneously doped channel one may express the drain current I_D as follows.

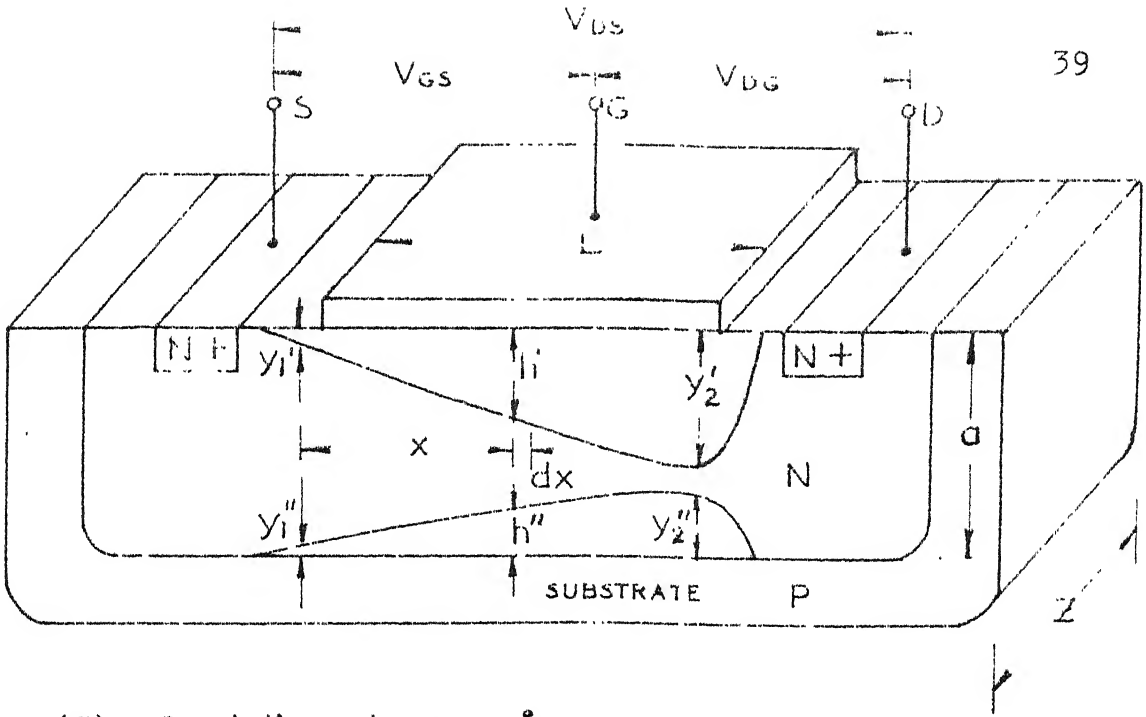
$$I_D = \frac{z\mu_o}{L} \int_{y_1}^{y_2} q\ N_o\ (a - h)\ h\ N_o\ q\ dh \quad .. \quad (3.1)$$

where the dimensions y_1, y_2 and h may be related to the dimensions shown in Figure 3.1(b) as

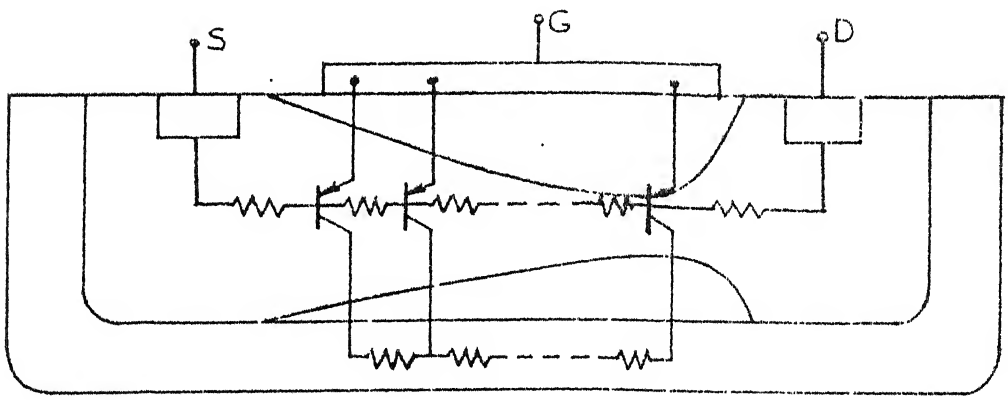
$$y_1 = y_1' + y_1'' \quad .. \quad (3.2)$$

$$y_2 = y_2' + y_2'' \quad .. \quad (3.3)$$

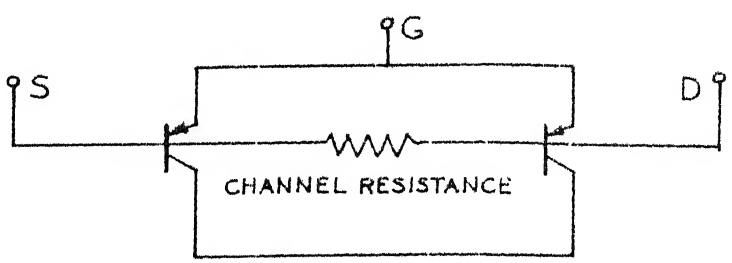
$$h = h' + h'' \quad .. \quad (3.4)$$



(a) Depletion layers in a JFET



(b) Parasitic transistors in JFET



(C) Equivalent parasitic element after lumping

FIGURE 3.1 JFET STRUCTURE AND PARASITIC ELEMENTS IN GRADUAL-CHANNEL OPERATION

Equation (3.1) may be expressed as

$$I_D = \frac{z\mu_o (N_o q)^2}{\varepsilon L} \left[\frac{a}{2} (y_2^2 - y_1^2) - \frac{1}{3} (y_2^3 - y_1^3) \right] \quad .. \quad (3.5)$$

It is evident from equation (3.5) that the channel current I_D depends on the total depletion layer heights at the source and drain point which is a consequence of the gradual-channel approximation. Therefore, one can lump the distributed parasitic elements into two transistors as shown in Figure 3.1(c). for evaluating the channel depletions y_1'' and y_2'' due to the effects of the substrate. The substrate-channel depletions may now be related as

$$y_1'' = \alpha_{FS}\, y_1' \quad .. \quad (3.6)$$

$$y_2'' = \alpha_{FD}\, y_2' \quad .. \quad (3.7)$$

where α_{FS} and α_{FD} are the values of the current gains of the two parasitic transistors at the source and drain ends respectively. The values of α_{FS} and α_{FD} are functions of the applied bias V_{GS} and V_{GD} respectively. The total depletions at the source and drain ends are therefore related as

$$y_1 = (1 + \alpha_{FS})\, y_1' \quad .. \quad (3.8)$$

$$y_2 = (1 + \alpha_{FD})\, y_2' \quad .. \quad (3.9)$$

where y_1' and y_2' are the depletion layer widths in the

channel due to gate-channel junction. Equation (3.5) can not be expressed explicitly in terms of the applied bias voltages V_{GD} and V_{GS} as the parameters α_{FS} and α_{FD} are not known due to the reasons stated in section 2.1.1. However, an interesting relationship may be obtained from equation (3.1) as follows.

The drain current I_D may be expressed as [3]

$$I_D\ (V_{GS},\ V_{GD}) = \int_{y_1}^{y_2} F(h)\ dh \qquad .. \quad (3.10)$$

which may be split into the two integrals as

$$I_D\ (V_{GS},\ V_{GD}) = \int_{o}^{y_2} F(h)\ dh - \int_{o}^{y_1} F(h)\ dh \quad .. \quad (3.11)$$

Using the same notation for I_D as in equation (3.10) one obtains equation (3.11) as

$$I_D\ (V_{GS},\ V_{GD}) = I_D\ (\ 0,\ V_{GD}) - I_D\ (0,\ V_{GS}) \qquad .. \quad (3.12)$$

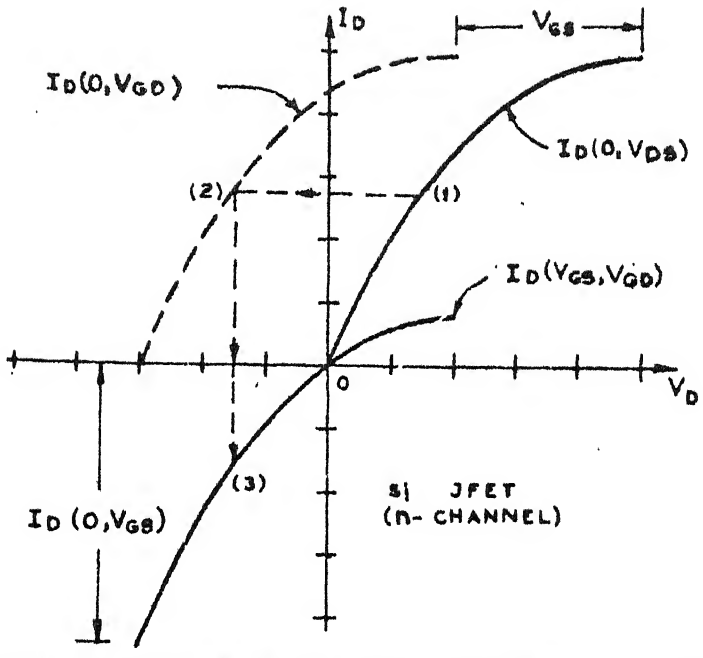
This relationship among the drain currents under different biasing condition is due to Wedlock [3] who has not considered the effect of substrate depletion. As it has been shown here, the equation relating the drain currents at different gate bias is also valid for planar JFET devices even when the effect of a floating substrate is taken into consideration. The validity of equation (3.12) may be used to check whether the gradual-channel approximation holds for a particular sample or not. It has indeed been found that among the samples tested in the

course of this work, none of the short-channel JFETs obeys the equation (3.12) while all the long-channel JFETs satisfy the equation.

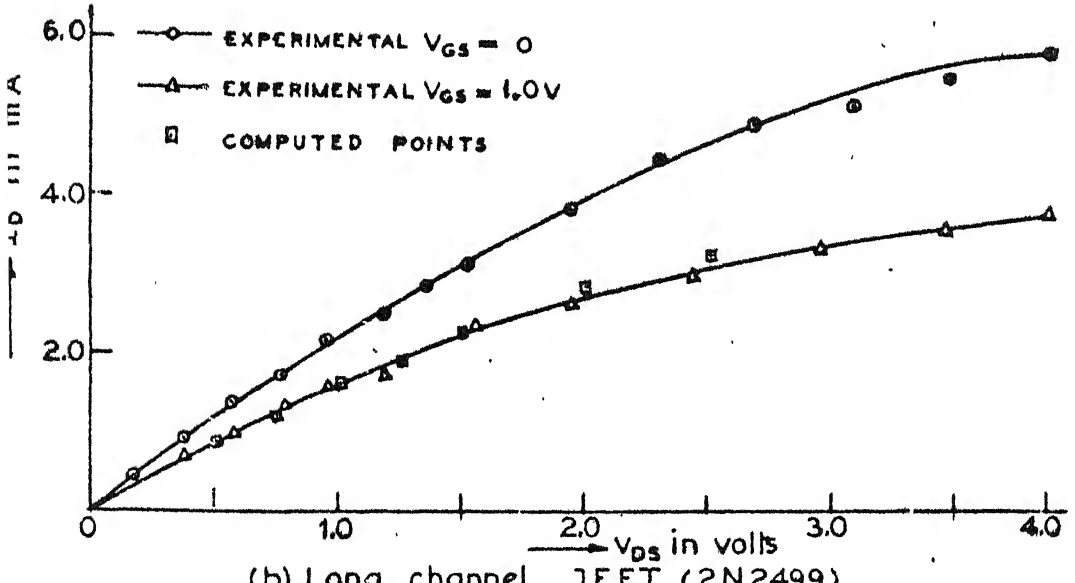
3.1.2. Test for validity of gradual channel approximation

A conventional setup for obtaining the $I_D - V_{DS}$ characteristic of a JFET for different values of V_{GS} can be used for this test. However, a pulsed $I_D - V_{DS}$ characteristic is preferred in order to maintain the temperature of the device constant and equal to that of the environment. The voltage to be applied between drain and gate should be in the range $-V_p < V_{GD} < 0$ for n-channel devices and $0 < V_{GD} < V_p$ for p-channel devices. So an a priori knowledge of pinchoff voltage V_p is essential.

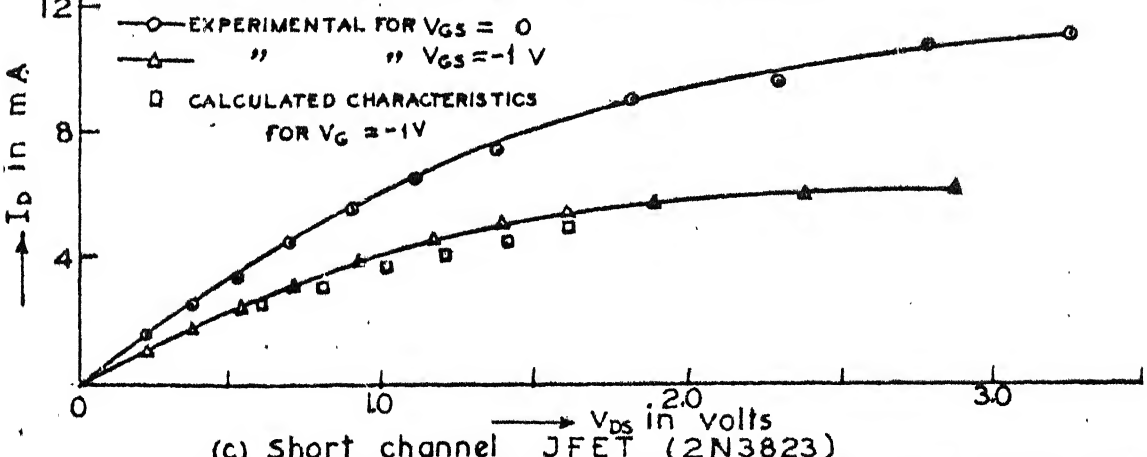
A plot of I_D (V_{GS}, V_{GD}) as a function of V_{GD} for any given value of V_{GS} can be obtained by a graphical construction based on equation (3.12) if a plot of I_D (0, V_{GD}) is experimentally obtained. This is illustrated in Figure 3.2(a). The Wedlock test consists simply of a comparison of this computed plot of I_D (V_{GS}, V_{GD}) with the one obtained from actual measurement. The natures of these plots for a typical long-channel and a typical short-channel JFET are shown in Figures 3.2(b) and (c) respectively.



(a) Graphical determination of I_D-V_{DS} characteristics of JFET



(b) Long channel JFET (2N2499)



(c) Short channel JFET (2N3823)

FIGURE 3.2 I_D-V_{DS} CHARACTERISTICS OF JFET IN GRADUAL CHANNEL OPERATION

3.1.3. Chiu-Ghosh Model for Short-channel JFETs

Chiu and Ghosh [4] have proposed a model for short-channel JFETs operating in the prepinchoff region. The two-section model as proposed by them is as follows.

i) The source section where the velocity of the carriers in the channel is less than the saturation velocity and

ii) The drain section where the velocity of the carriers in the channel attains the saturation value.

According to the model, the drain current I_D is related to the drain voltage V_{DS} and the gate voltage V_{GS} as

$$I_D = \frac{k\, I_s}{V_{DS} + k \frac{v_s L}{\mu_o}} \left[V_{DS} - \frac{2}{3} \frac{1}{\sqrt{V_p + V_{bi}}} \right.$$

$$\left. \left\{ (-V_{GS} + V_{DS} + V_{bi})^{3/2} - (-V_{GS} + V_{bi})^{3/2} \right\} \right] \quad .. \quad (3.13)$$

where k and I_s are given by the expressions

$$k = \frac{\mu_o E_o}{\mu_o E_o + v_s} \quad .. \quad (3.14)$$

$$I_s = q\, N_o\, a z v_s \quad .. \quad (3.15)$$

v_s is the saturation velocity of the carriers in the channel and E_o is the magnitude of the threshold electric field for velocity saturation. Equation (3.13) may be written as

$$\frac{1}{I_D}\left[V_{DS} - \frac{2}{3}\frac{1}{\sqrt{V_p + V_{bi}}}\left\{(-V_{GS} + V_{DS} + V_{bi})^{3/2} - (-V_{GS} + V_{bi})^{3/2}\right\}\right] = \frac{V_{DS}}{kI_s} + \frac{1}{g_o} \qquad .. \quad (3.16)$$

where the equation (2.12) for g_o has been substituted. Let the left side of equation (3.16) be designated as $F(I_D, V_{DS}, V_{GS})$. Then, one expects a linear relationship of $F(I_D, V_{DS}, V_{GS})$ with respect to V_{DS}, whose slope and intercept on the y axis should be $\frac{1}{kI_s}$ and $\frac{1}{g_o}$ respectively. With this idea, an experimental verification of equation (3.16) has been done with a typical sample of short-channel JFET type 2N 3823. The values of V_p and V_{bi} have been measured from the plot of g_{do} vs V_{GS} and obtained as 2.75 volts and 0.425 volts respectively. Table 3.1 lists the experimental data, the value of $F(I_D, V_{DS}, V_{GS})$ for each observation. V_{GS} has been kept zero for all observations.

TABLE 3.1

V_{DS}	I_D	F (I_D, V_{DS}, V_{GS})
0.4 v	2.4 mA	92.75
0.8 v	4.4 mA	89.725
1.2 v	6.0 mA	87.662
1.5 v	7.0 mA	85.83
1.75 v	7.5 mA	86.56
2.0 v	8.0 mA	85.7

The table clearly shows that the plot of F (I_D, V_{DS}, V_{GS}) can not be linear with respect to V_{DS}. The validity of the model is thus questionable and it has not been included in further deliberations.

3.2. Circuit parameters from gradual-channel model

There are two conductances and one capacitance available from the operation of the device in this mode. The device parameter relationships as obtained through them are shown in the following subsections.

3.2.1. Conductances in the gradual channel model

Equation (3.5) may be written as

$$I_D = g_o \left[V_{DS} - \frac{2}{3} \frac{1}{\sqrt{(V_p + V_{bi})}} (-V_{GD} + V_{bi})^{3/2} + \frac{2}{3} \frac{1}{\sqrt{V_p + V_{bi}}} (-V_{GS} + V_{bi})^{3/2} \right] \quad .. \quad (3.17)$$

where the effect of the substrate has been ignored. The expressions for g_{ds} and g_m are given by direct differentiation :

$$g_{ds} = \frac{\delta I_D}{\delta V_{DS}} = g_o \left[1 - \sqrt{\left(\frac{-V_{GD} + V_{bi}}{V_p + V_{bi}} \right)} \right] \quad .. \quad (3.18)$$

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{g_o}{\sqrt{V_p + V_{bi}}} \left[\sqrt{(-V_{GD} + V_{bi})} - \sqrt{(-V_{GS} + V_{bi})} \right] \quad .. \quad (3.19)$$

Thus the values of g_o and V_p may be determined from these two equations.

3.2.2. Input capacitance of JFET

The input capacitance of a JFET under common source is given as [5]

$$c_{iss} = \frac{\varepsilon z}{a} \int_o^L \frac{dx}{y(x)} \quad .. \quad (3.20)$$

where y(x) is the depletion width expressed as a function of the distance x measured from source along the channel. Equation (3.1) and (3.20) may be combined to obtain an expression for c_{iss} as follows (see appendix A - 1 for derivation).

$$\frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \left[1 - \frac{2}{3} \frac{u_2^2 + u_1 u_2 + u_1^2}{u_1 + u_2} \right] \quad .. \quad (3.21)$$

where u_1 and u_2 are the square root of the normalised voltages at the source and drain ends of the channel respectively.

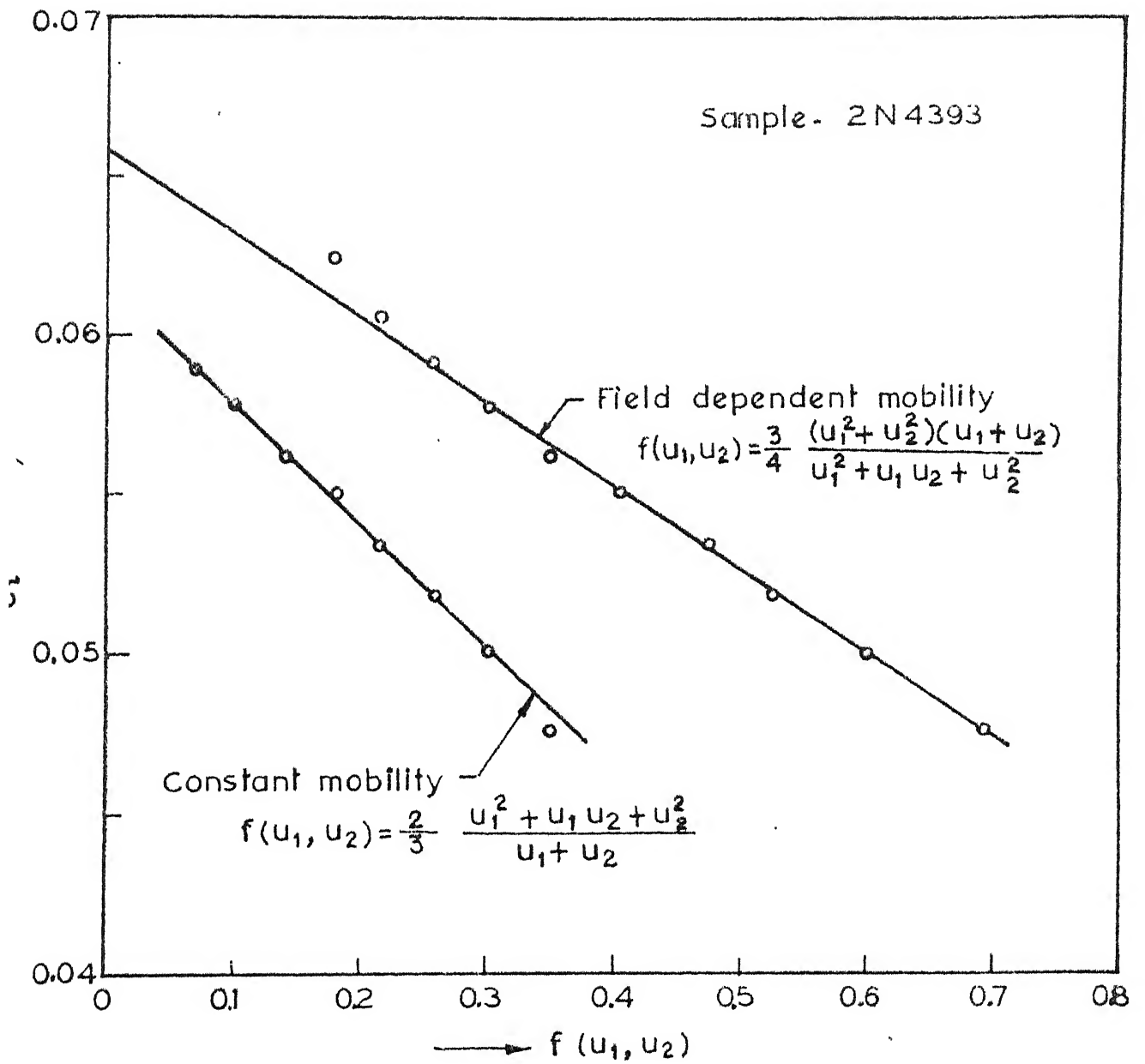


FIGURE 3.3 PLOT OF $\frac{1}{C_{ISS}}$ Vs. $f(u_1,u_2)$

3.3. Device parameter relationships

The following combinations of the device parameters can thus be obtained from gradual-channel model for long-channel JFETs.

i) Open channel conductance g_o

ii) Pinchoff voltage V_p

iii) Value of $\frac{a}{\varepsilon z L}$

It may be pointed out that due to discrepancy in the model for c_{iss}, it will be preferable to use the model of c_g in the parallel-channel region where there is no ambiguity. Besides, the device parameter combination $\frac{a}{\varepsilon z L}$ may also be evaluated from parallel-channel measurements with the knowledge of the pinchoff voltage and the slope of $\frac{1}{c_g^2}$ vs V_{GS} characteristics. Therefore c_{iss} is left out of further consideration.

The expressions for g_{ds} and g_m involve g_o and V_p, the two parameters already obtained from parallel-channel model. In gradual-channel model, these parameters are obtained only for long-channel JFETs with the help of the gradual-channel approximation, whereas no such consideration need be evoked for obtaining g_o and V_p from parallel-channel measurements. Hence the value of g_o and V_p will not be determined from gradual-channel measurements. Thus one

observes that this mode of operation does not contribute towards any more relationships involving device parameters other than those already obtained from the parallel-channel model. However, this mode of operation does offer a method for ascertaining whether a device is long-or short-channel, based on direct circuit measurement. This test is applied to every JFET under consideration before proceeding with any post-pinchoff measurements in chapter 4.

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CHAPTER - IV

POST - PINCH OFF MODELS

Gradual channel behaviour of JFET has been analysed with the approximation introduced by Shockley [1], which allowed the decomposition of inherently two-dimensional nature of the continuity and Poisson equation in two one-dimensional problems. This gradual-channel approximation is no longer valid for JFET operation in the post-pinch off region. Hence, one has to employ numerical techniques for the solution of the two-dimensional coupled equations [2] outlined in Chapter 1. These numerical solutions are not directly useful in the construction of models due to their complexity. However, guided by these numerical solutions, several workers have attempted different approximations which have led to the development of a large number of models for the post-pinch off operation of JFETs. All such approximations involve the three basic steps :

i) partitioning of the entire channel into different regions,

ii) solutions of the equations in each region within certain assumptions, and

iii) matching of the solutions between adjacent

regions through suitable criteria at the interface.

The exact nature of each of these steps depends on the objective of the model and will therefore be elaborated in connection with the specific models considered later in this chapter. Table 4.1 lists some of the models to present a brief overview.

The post-pinchoff region is by far the most widely used region of JFET characteristics, the most common use being in amplifiers. As such, a standard two-port model, shown in Figure 1.2(d) has been well-established for this mode of operation. The parameters of the equivalent circuits are :

(i) g_m, (ii) r_{ds}, (iii) c_{gs}, (iv) c_{gd} and (v) c_{ds}.

The experimental methods for the measurement of most of these parameters are well-known and the typical values of these parameters are also often published by different manufacturers. With the objective of the present work in mind, one should, therefore, consider only those physical models which yield reliable expressions for all or some of these circuit parameters in simple and closed mathematical forms. It may be added that one would look for expressions for the magnitudes of the measurable circuit quantities like I_D, V_{GS}, V_{DS} and V_{Dp} in terms of the different device parameters in the different models.

Table 4.1. Post-pinchoff Models of JFET.

Year of Publication	Total No. of regions in the channel	Matching criteria of the Solutions at the interface of two adjacent regions.	Remarks on usability in the present Work
1967	Three	Potential, potential gradient and drain conductance.	Solution available in implicit algebraic form and not usable for that reason.
1968	Three	Potential, Potential Gradient and charge density.	Solutions does not connect device parameters and circuit parameters directly and is not very useful.
1969	Three	Electric field E_x is matched at the boundary. The excess channel charge is assumed to meet this criteria.	Solutions are simple and algebraic relationships between device parameters and circuit parameters are available and useful.
1970	Three	Electric field is matched at the interface with field dependent mobility.	Solutions involve auxiliary parameters which are difficult to eliminate and are not very useful
1975	Four	The three regions of Grebene and Gandhi along with a fringe region where the electric field in both direction is the criteria for obtaining the fringe region.	Solution is accurate, but mathematically cumbersome. Provides a good insight into the phenomenon of saturation and a basic understanding on the device operation

Both the Grebene-Gandhi and the Lehovec-Miller models do satisfy these requirements, the latter being an improvement on the former. The Lehovec-Miller model has the advantage of being able to draw valuable information from the accurate numerical solutions obtained by Kennedy and O'brien [8]. As borne out by the experimental measurements discussed later, the expressions for the circuit parameters derived from the Lehovec-Miller model are the best fits for the experimental values known to date. The model provides the relationships between I_D, V_{DS}, V_{GS} in the post-pinchoff region which have been utilised in deriving the expressions for the different circuit parameters. After a brief discussion of the Grebene-Gandhi model, therefore the Lehovec-Miller model is studied in detail for the purpose of obtaining relationships of the circuit parameters and the device parameters in the post-pinchoff operation of JFETs.

In this context, it may be noted that both the models have been derived on the basis of gradual-channel approximation, hence they are only applicable to long-channel devices.

4.1. Grebene - Gandhi model [5]

Grebene and Gandhi have considered a third region in addition to the two regions used by Shockley [1] for the gradual-channel operation of JFETs as shown in

Figure 4.1. In the conducting channel within this third region carrier velocity is always equal to the saturation velocity irrespective of the field within this section of the channel, and channel current continuity is maintained through generation of excess carriers within this region, a fact supported by the numerical solution of the device equations. The matching at the interface of the gradual-channel region and this region of velocity saturation is based on the continuity of the electric field along the channel. The drain voltage V_{Dp} in excess of the pinchoff voltage V_p, appears across the space-charge layer created in the conducting channel, leading to the saturation of the drain current I_D.

4.2. Lehovec-Miller model [7]

Lehovec and Miller have pointed out the following inadequacies of the Grebene-Gandhi model:

i) The fringing effect of the depletion layer at the drain end has not been considered although the phenomenon is well-known from numerical results obtained through a rigorous solution of the basic device equations.

ii) The excess carrier generation in the channel is assumed without any consideration for the electro-neutrality of the channel.

The model proposed by Lehovec and Miller takes care of these two inadequacies through the con[illegible]

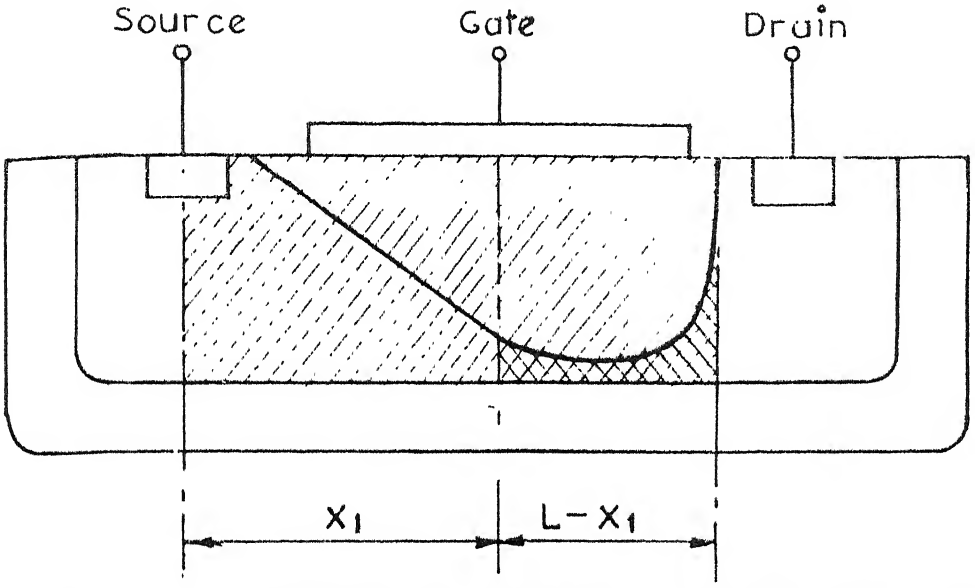


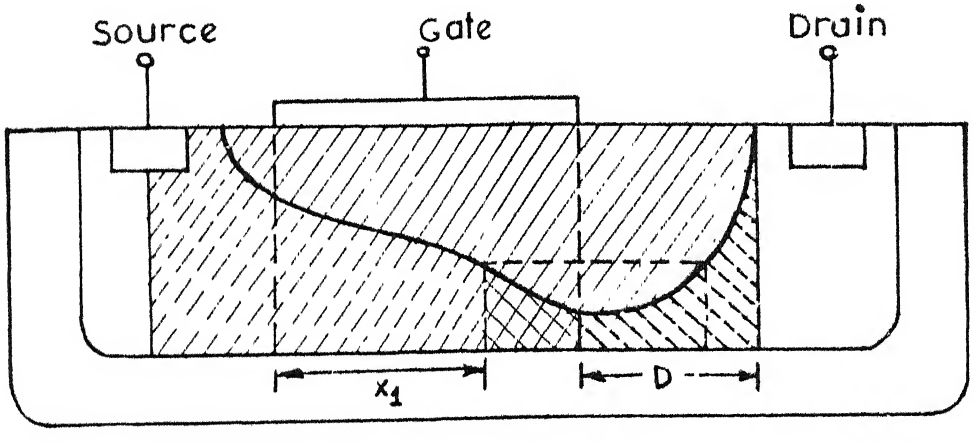
FIGURE- 4.1 DIFFERENT REGIONS WITHIN THE CHANNEL IN GREBENE - GANDHI MODEL

Depletion region I

Gradual channel region II

Velocity saturation region III

Fringe region IV



IGURE- 4.2 DIFFERENT REGIONS WITHIN THE CHANNEL IN LEHOVEC-MILLER MODEL

of a fringe region within the channel as shown in figure 4.2. The velocity-saturation region of the Grebene-Gandhi model has been extended upto the end of the gate on the drain side. For consideration of this electrostatic fringing effect, a line charge at this end of the gate is assumed. The density of this line charge has been calculated through the matching of the electric field at the interface of the velocity-saturated and the fringe regions. The model ensures the electro-neutrality of the gate-channel junction and the residual channel independently, the latter requirement giving rise to a dipole layer in the residual channel near the drain contact.

The model provides the following expression for V_{Dp}, the potential difference across the velocity saturated region and the fringe region taken together.

$$V_{Dp} = \frac{2k\ (V_p + V_{bi})}{\pi} \left[\sinh \frac{\pi(L - x_1)}{2a} + \frac{D}{ak} \ln \left(\cosh \frac{\pi D}{2a}\right)\right] \quad .. \quad (4.1)$$

where
$$D = ak \cosh \frac{\pi(L - x_1)}{2a} \quad .. \quad (4.2)$$

and
$$k = \frac{a\mathcal{E}_o}{V_p + V_{bi}} \quad .. \quad (4.3)$$

D is the extension of the depletion region beyond gate

edge as shown in Figure 4.1 and x_1 is the length of the section of the channel from the source end to the point at the onset of velocity saturation. In other words, x_1 is the length of the graaual-channel section. The parameter k is a dimensionless quantity implying the degree of velocity saturation in the conducting channel. E_o is the threshold electric field for velocity saturation.

From equations (4.1) and (4.2) it is obvious that the length of the velocity-saturated region $(L - x_1)$ and the length of the fringe region D depend on V_{Dp} and not on the drain current I_D. The drain current I_D is given by

$$I_D = N_o q \, v_s \, z b_1 \qquad .. \quad (4.4)$$

where b_1 is expressed as

$$b_1 x_1 = \frac{a^2}{3k} \left[1 - 3 \left(\frac{b_1}{a}\right)^2 + 2 \left(\frac{b_1}{a}\right)^3 - 3w^2 + 2w^3 \right] \qquad .. \quad (4.5)$$

w is the non-dimensional depletion layer height and is given by

$$w = \sqrt{\frac{|V_{(x)}| + V_{bi}}{V_p + V_{bi}}} \qquad .. \quad (4.6)$$

It may be noted that although the expressions given above are somewhat involved, they are in a closed mathematical form and are explicit in the sense that the magnitude of V_{Dp} can be computed for any value of I_D by

using equations (4.1) to (4.6), provided the values of the device parameters N_D, a, z, L and the value of v_s are known together with that of V_{GS}. Using the published values of $\frac{L}{a}$ [5] of 2N2499, this procedure has been followed for computing the characteristic of V_{DS} against normalised drain current in the post-pinchoff region shown in Figure 4.3; the experimentally measured values of I_D and V_{DS} for the same JFET are also indicated in the figure clearly bringing out the validity of the model.

Table 4.2 lists the values of $\frac{b_1}{a}$ and $\frac{\pi(L - x_1)}{2a}$ obtained in the course of the computation of V_{DS} for different values of $\frac{b_1}{a}$. It is obvious from an examination of the data that

$$\frac{b_1}{a} < 0.04 \text{ for } \frac{V_{Dp}}{V_p} \leqslant 58 \qquad .. \quad (4.7)$$

and

$$(1 - \frac{x_1}{L}) < 0.1 \quad \text{for} \quad \frac{V_{Dp}}{V_p} \leqslant 6.0 \qquad .. \quad (4.8)$$

The inequality (4.7) permits equation (4.5) to be approximated as follows for the entire usable range of the device characteristics. Therefore, one may obtain the expression

$$b_1 x_1 \simeq \frac{a^2}{3k} [\, 1 - 3w^2 + 2w^3 \,] \qquad .. \quad (4.9)$$

Equations (4.4) and (4.9) lead to the basic relationship

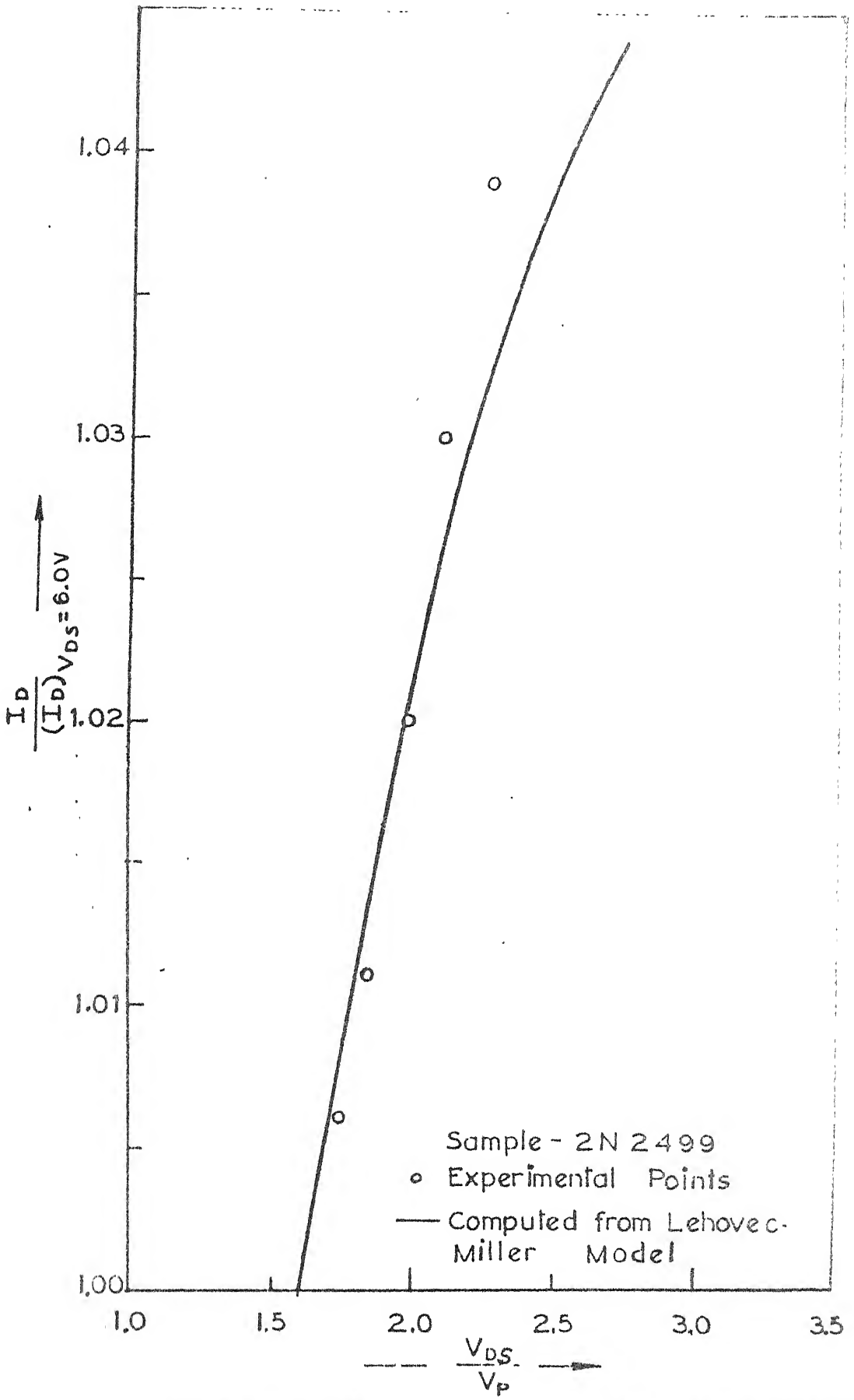


FIGURE 4.3 COMPARISON OF EXPERIMENTAL AND COMPUTED (L-M) MODEL $I_D - V_{DS}$ CHARACTERISTICS

$$I_D x_1 = \frac{N_o q v_s z a^2}{3k} [\ 1 - 3w^2 + 2w^3\ ] \quad .. \quad (4.10)$$

Equation (4.10) will be utilised in the following sections to obtain expressions for the circuit parameters in the post-pinchoff operation of the device.

Table 4.2

Computed values of $\frac{b_1}{a}$, $\frac{x_1}{L}$, $\frac{D}{L}$ and $\frac{V_{DS}}{V_p}$ for 2 N 2499.

$\frac{b_1}{a}$	$\frac{x_1}{L}$	$\frac{D}{L}$	$\frac{V_{DS}}{V_p}$
0.0318	0.998	0.095	1.531
0.032	0.991	0.096	1.61
0.033	0.958	0.116	2.29
0.034	0.926	0.165	3.86
0.035	0.897	0.248	7.502
0.036	0.869	0.375	15.73
0.037	0.843	0.564	33.90
0.038	0.824	0.753	59.17

If one neglects the effect of fringing on the drain side of the gate, that is the extension of the depletion layer beyond the gate edge on the drain side is ignored, the quantity D is set equal to zero. Then,

for low values of V_{Dp} ($V_{Dp} \leqslant 6.5\ V_p$) one has the following approximate expression

$$V_{Dp} \simeq (L - x_1)\ E_o \qquad .. \quad (4.11)$$

The expression given by equation (4.11) is identical with the expression obtained by Grebene and Gandhi [5] for small values of applied drain-source bias beyond pinchoff.

4.3. Relationships between device parameters and Circuit parameters

The relationships of the different circuit parameters in the post-pinchoff region of operation of JFET have been derived from the Lehovec-Miller model. Rigorous relationships have been developed for each of the circuit parameters and have been approximated for the sake of comparison with the relationships obtained from other models.

4.3.1. Mutual conductance of the JFET

The length of the gradual channel section x_1 as shown in Figure 4.2 is independent of V_{GS} and the quantity $I_D x_1$ is independent of V_{DG} as shown in equation (4.10). Mutual conductance g_m may now be defined as

$$g_m = \left.\frac{\delta I_D}{\delta V_{GS}}\right|_{V_{DG}\ \text{is constant}} \qquad .. \quad (4.12)$$

Substituting equation (4.10) for I_D, one obtains

$$g_m = \frac{1}{x_1} \frac{d\ (I_D x_1)}{d\ V_{GS}} \qquad .. \quad (4.13)$$

wherefrom g_m is given by

$$g_m = \frac{N_o q v_s\ az}{x_1\ E_o} (1 - w) \qquad .. \quad (4.14)$$

Again substituting equation (4.4) in (4.14) the following expression is obtained

$$\frac{I_D}{g_m} = \frac{V_p + V_{bi}}{3(1 + 2w)(1 - w)} \qquad .. \quad (4.15)$$

The expression for g_m as given by equation (4.14) is very close to the expression provided by Grebene and Gandhi as follows

$$g_m \simeq \frac{N_o q a z\ v_s}{x_1\ E_o} + \frac{1}{r_{ds}} \qquad .. \quad (4.16)$$

Equation (4.16) does not show the functional dependence of g_m on V_{GS} which has been obtained in equation (4.14). The original model of Shockley also gives rise to an expression similar to equation (4.14). However, it may be pointed out that the model for the circuit parameter g_m is not very well fitted to the experimental results; Middlebrook and Richer [9] have provided the following empirical relationship.

$$I_{DS} = I_{DSS}\ (1 - \frac{V_{GS}}{V_p})^n \qquad .. \quad (4.17)$$

where the index n lies in the neighbourhood of 2. This

empirical expression has been found to agree with experimental results indicating an altogether different expression for g_m. Moreover, the dependence of g_m on V_{GS} as suggested by equation (4.15) does not follow the one obtained from equation (4.17). Hence, it may be concluded that the existing post-pinchoff models for JFET are not quite competent in explaining the functional dependence of the circuit parameter g_m. Besides, this parameter does not bring out values for any combination of device parameters except pinch-off voltage, which may be obtained from other reliable models. Hence, this circuit parameter will not be pursued in future work.

4.3.2. Incremental drain-source resistance r_{ds}

Drain-source incremental conductance g_{ds} may be defined as

$$g_{ds} = \left.\frac{\delta I_D}{\delta V_{DS}}\right|_{V_{GS} \text{ is constant}} \quad .. \quad (4.18)$$

It is known from equation (4.10) that

$$\left. d(I_D\, x_1) \right|_{V_{GS} = \text{constant}} = 0 \quad .. \quad (4.19)$$

so that,

$$I_D \frac{dx_1}{dV_{DS}} = - x_1 \frac{dI_D}{dV_{DS}} \quad .. \quad (4.20)$$

and as a result

$$I_D\, r_{ds} = x_1\, E_o \quad .. \quad (4.21)$$

is obtained with the help of equation (4.11). Equation

(4.21) may be further approximated with the help of the inequality (4.8) as

$$I_D\, r_{ds} \simeq LE_o \qquad .. \quad (4.22)$$

The equations suggested by Grebene and Gandhi for $I_D\, r_{ds}$ are given below.

$$I_D\, r_{ds} = x_1 E_o \cosh \frac{\pi(L - x_1)}{2a} \qquad .. \quad (4.23)$$

and

$$I_D\, r_{ds} \simeq LE_o \cosh \frac{\pi(L - x_1)}{2a} \qquad .. \quad (4.24)$$

A comparison between the equations (4.21) and (4.23), and the equations (4.22) and (4.24) reveals the fact that for small V_{Dp}, the equations are not different with respect to each other, provided the inequality (4.8) is obeyed. However, a near exact derivation for $I_D\, r_{ds}$ for large V_{Dp} from the equations obtained in the Lehovec-Miller model gives rise to the following expression.

$$I_D\, r_{ds} = x_1 E_o \cosh \frac{\pi(L-x_1)}{2a} \left[1 + \tanh \frac{\pi(L-x_1)}{2a} \right.$$

$$\left. \left\{ \ln \cosh \frac{\pi D}{2a} + \frac{D}{2a} \tanh \frac{\pi D}{2a} \right\} \right] \qquad .. \quad (4.25)$$

Equation (4.25) may be approximated in the form of the equation (4.23) for small values of $\frac{V_{Dp}}{V_p}$. The validity of the equations has been discussed further in section 4.4.1

4.3.3. Post-pinchoff capacitances in JFET

The presence of a dipole layer due to space-charge accumulation and inversion within the residual channel has been obtained through the numerical solution [8]. Lehovec-Miller model has provided a first order differential equation for calculation of this channel space-charge at different bias voltages. The equation is not integrable in a closed mathematical form. On the other hand, field plotting for evaluation of the capacitances within the depletion region and the residual channel is a fairly involved task as it leads ultimately to root evaluation of transcendental functions near singular points. So, modelling of the capacitances of JFET in post-pinchoff region is rather difficult. However, a novel approach has been found to be helpful for this purpose and is described below.

The capacitances of the usual three terminal JFET device are three in number . The two capacitances arising out of the depletion layer charge between gate and channel are defined as c_{gs} and c_{gd}, capacitances between gate and source and gate and drain terminals respectively. The other capacitance c_{ds} is due to the accumulation and inversion of the space-charge within the residual channel and is present across the drain and source terminals of the device. The capacitances and their inter-connections have been shown in Fig.1.2(d).

It may be noted that c_{gs} and c_{gd} are the two capacitances which are formed due to the presence of a single gate-channel depletion layer; one has to evolve a criterion such that the total depletion layer charge may be divided into two components dependent on V_{GS} and V_{GD} respectively. Then one can define

$$c_{gs} = \frac{\delta Q_g}{\delta V_{GS}} \Bigg|_{V_{GD} \text{ is constant}} \quad .. \quad (4.26)$$

and

$$c_{gd} = \frac{\delta Q_g}{\delta V_{GD}} \Bigg|_{V_{GS} \text{ is constant}} \quad .. \quad (4.27)$$

Figures 4.4(a) and (b) show the excess charges δQ_{gs} and δQ_{gd} due to small changes in V_{GS} and V_{GD} respectively. Figure 4.4(c) shows the entire depletion layer charge Q_g and the associated dimensions for its calculation. Q_g may be expressed as

$$Q_g = N_o q z \left[a\,(L+D) - \frac{x_1}{2}\right] b_o \quad .. \quad (4.28)$$

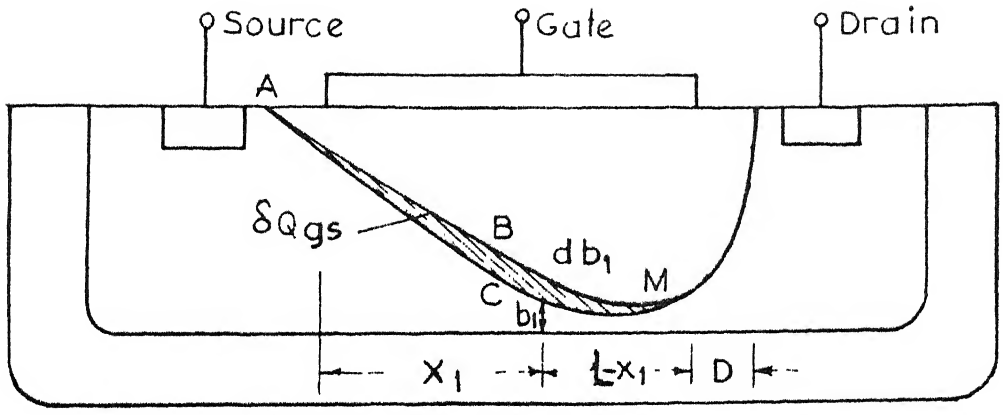
where b_o is the residual channel height at the source end and may be expressed as

$$b_o = a(1 - w) \quad .. \quad (4.29)$$

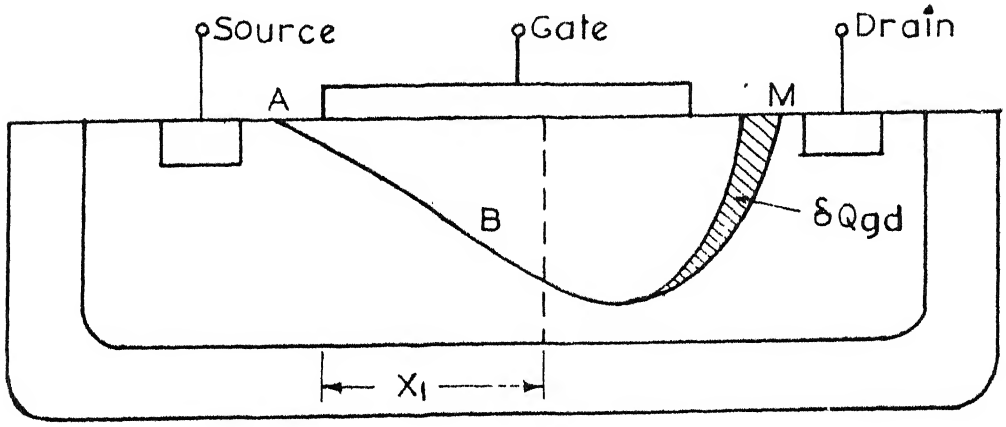
where

$$w = \sqrt{\frac{|V_{GS}| + V_{bi}}{V_p + V_{bi}}} \quad ..$$

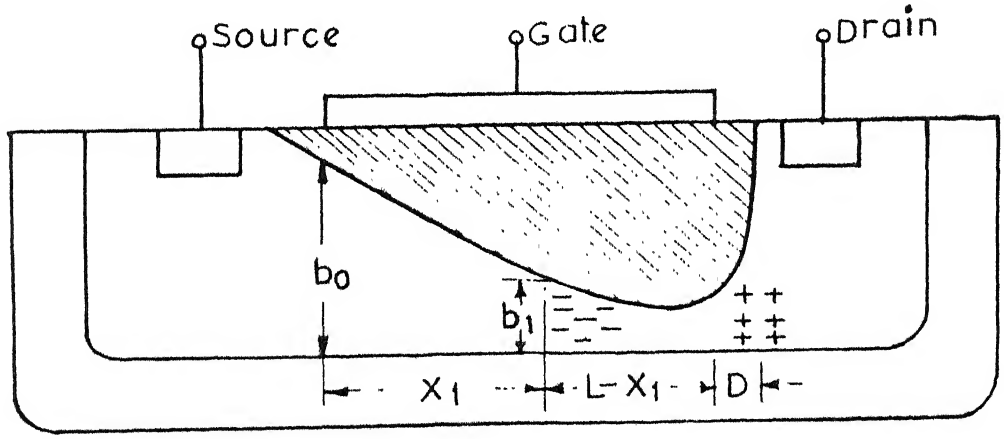
is the non-dimensional depletion layer width at the source end. From equations (4.2) and (4.5) it is obvious that the quantities D and x_1 do not depend on V_{GS}



(a) Excess charge in gate channel depletion layer to variation of V_{GS}



(b) Excess charge in gate channel depletion layer due to variation of V_{GD}



(c) Total depletion layer charge within the depleted channel and the dipole layer in residual channel

FIGURE-4.4 CHARGE DISTRIBUTION IN JFET CHANNEL

whereas b_o depends on V_{GS}; likewise, D and x_1 depend on V_{GD} whereas b_o is independent of V_{GD}. Therefore, one may obtain expressions for c_{gs} and c_{gd} as

$$c_{gs} = \frac{\delta Q_g}{\delta b_o} \cdot \frac{\delta b_o}{\delta V_{GS}} \Bigg|_{V_{GD} = \text{constant}} \quad .. \quad (4.30)$$

and

$$c_{gd} = \frac{\delta Q_g}{\delta x_1} \cdot \frac{\delta x_1}{\delta V_{GD}} \Bigg|_{V_{GS} = \text{constant}} \quad .. \quad (4.31)$$

Equation (4.30) may be rewritten after the necessary substitutions and simplifications as

$$c_{gs} = \frac{2 \varepsilon z x_1}{aw} \quad .. \quad (4.32)$$

Combining with equations (4.4) and (4.5) one obtains

$$c_{gs} = \frac{\varepsilon z^2 \mu_o (V_p + V_{bi}) N_o q [1 - 3w^2 + 2w^3]}{6 w I_D} \quad .. \quad (4.33)$$

which may be rewritten as

$$c_{gs} = \frac{L^2 g_o^2}{12 \mu_o I_D} \left[\frac{1}{w} - 3w + 2w^2 \right] \quad .. \quad (4.34)$$

where g_o is the open-channel conductance.

So, c_{gs} is independent of V_{GD} for given values of V_{GS} and I_D. Table 4.3 shows this independence as well as the dependence on I_D.

TABLE 4.3

Experimental data for c_{gs} (Sample 2 N 2498)

V_{GD} in volts	I_D in mA	c_{gs} in pf
2.0	1.0	8.05
4.0	1.0	8.05
7.0	1.0	8.05
4.0	2.0	8.46
4.0	3.0	8.68
4.0	4.0	8.82
4.0	5.0	9.00
4.0	6.0	9.12

The plot of $I_D\, c_{gs}$ against $\left(\frac{1}{w} - 3w + 2w^2 \right)$ is shown in Figure 4.5. The plot is almost linear.

An expression for c_{gd} may be written from equation (4.31) as follows

$$c_{gd} = N_o qaz \left[\frac{d}{dx_1} D - \frac{b_o}{2a} \right] \cdot \frac{dx_1}{dV_{Dp}} \qquad .. \quad (4.35)$$

one can use equation (4.1) and (4.2) for obtaining the derivatives required in equation (4.35). Thus, an expression for c_{gd} may be developed, but its functional dependence on V_{Dp} can not be separated from the device parameters. Table 4.4 lists the experimental data for

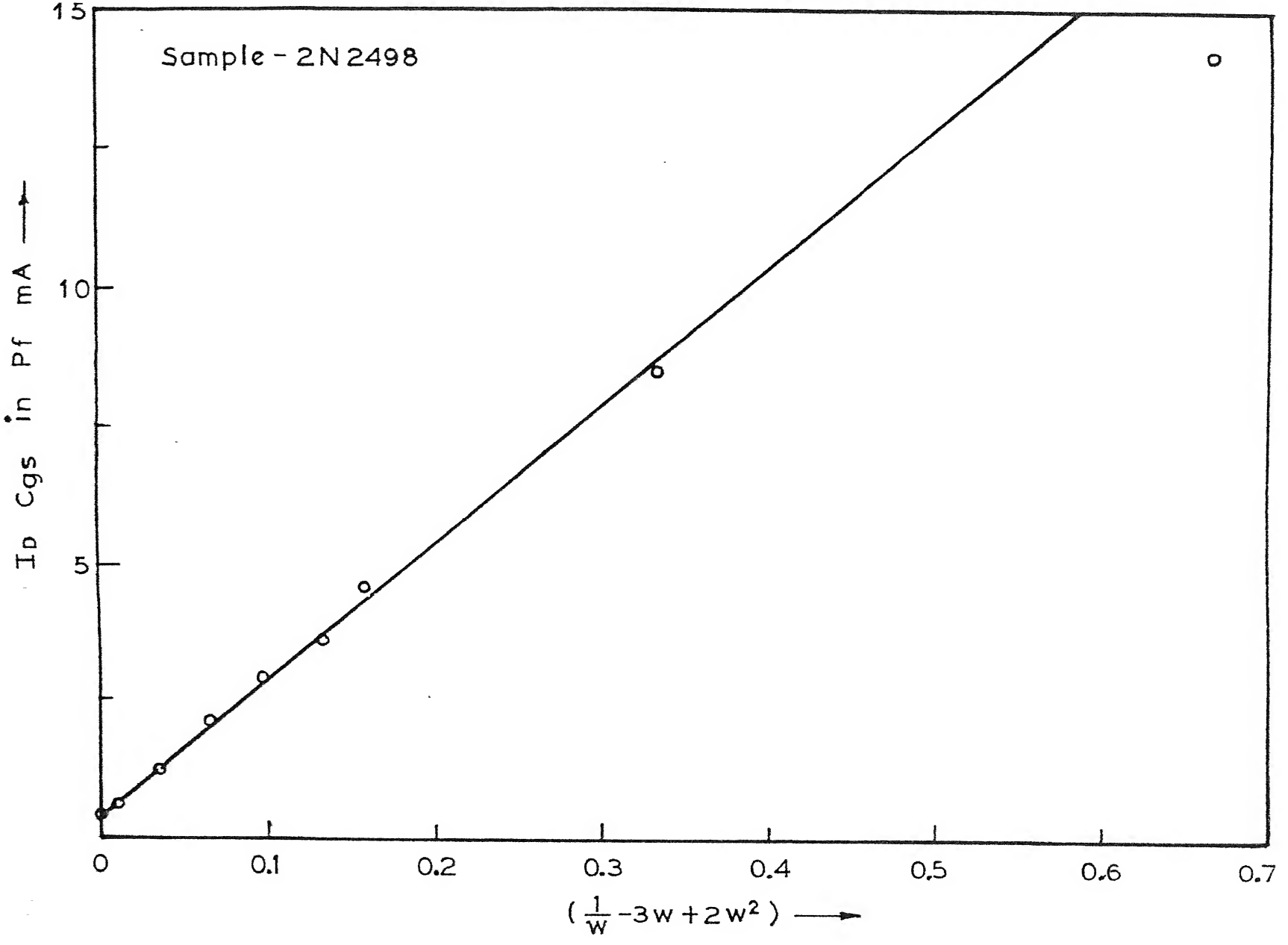


FIGURE - 4.5 PLOT OF I_D Cgs Vs $(\frac{1}{W} - 3W + 2W^2)$

c_{gd} with variation of V_{Dp} and I_D (consequently V_{GS}). It is interesting to note that c_{gd} has a very weak dependence on I_D, but it changes with change of V_{DG}. This ensures the previous assumptions in its derivation.

TABLE 4.4

Experimental data for c_{gd} (Sample 2N 4393)

V_{DG} in volts	I_D in mA	c_{gd} in pf
2.0	1.0	5.5
3.0	1.0	4.78
4.0	1.0	4.38
5.0	1.0	4.00
6.0	1.0	3.86
7.0	1.0	3.62
6.0	0.2	3.80
6.0	0.4	3.78
6.0	0.6	3.76
6.0	1.2	3.75

c_{gd} is not a circuit parameter of interest for the present work and therefore the expression and its experimental validation has not been pursued.

Misra and Prasad [10] have evolved an over-simplified model from Grebene-Gandhi model for the drain-source capacitance c_{ds}. According to them the

variation of a space-charge in the residual channel, due to a change in applied drain-source bias is the basis of this capacitance. But, in formulation, the portion of the channel bounded by the length x_1 from the source and the drain end has been assumed by Misra and Prasad, where the charge density due to the gate-channel depletion layer has been considered as shown in Figure 4.4(c). Further, they have improperly considered c_{ds} as a parallel-plate capacitance with area 'az' and distance $L-x_1$, which indicates that c_{ds} is caused by depletion layer charge. According to their treatment;

$$c_{ds} = \frac{\varepsilon a z}{L-x_1} \qquad .. \quad (4.36)$$

where $(L-x_1)$ is again substituted from Grebene-Gandhi model. The final form of the expression for c_{ds} as obtained by them is given below :

$$c_{ds} = \frac{\pi \varepsilon z}{2 \sinh^{-1}\left(\frac{\pi V_{Dp}}{2aE_o}\right)} \qquad .. \quad (4.37)$$

A further simplification imposed by them for $|V_{Dp}| << V_p$ yields

$$c_{ds} = \frac{\pi \varepsilon z}{2 \ln\left(\frac{\pi V_{Dp}}{aE_o}\right)} \qquad .. \quad (4.38)$$

Hence a plot of $\frac{\pi\varepsilon}{2c_{ds}}$ against $\ln \frac{\pi V_{Dp}}{V_p}$ should yield the value of $\ln\left(\frac{aE_o}{V_p}\right)$ as intercept on y-axis and z as the reciprocal of the slope.

Equation (4.38) does not appear to be ~~quite~~ correct due to the violation of the basic property of electroneutrality over a dipole layer giving rise to capacitive effect in a circuit. Therefore, the model is rather unreliable.

4.4. Experimental measurement of circuit parameters

Post-pinchoff measurements of circuit parameters are not very simple due to the fact that the circuit parameters are to be measured as per their definition. So, incremental measurements are required for each of the parameters. In the following subsections, the technique of measurements developed during the course of this work are presented.

4.4.1. Measurement of r_{ds}

Equation (4.24) may be rewritten as

$$(I_D r_{ds})^2 = L^2 E_o^2 + \left(\frac{\pi V_{Dp} L}{2a} \right)^2 \qquad .. \quad (4.39)$$

This equation suggests that a plot of $(I_D r_{ds})^2$ against $\pi^2 V_{Dp}^2$ should be linear with a slope of $\frac{L^2}{4a^2}$. An experimental verification of the relationship has been carried out by the measurement of r_{ds} as described below.

The measurement in the post-pinchoff region calls for a considerable power dissipation within the device. In order to ensure that the temperature of the device is

the same as the ambient temperature a pulsed measurement has been done. The set up for this experiment is shown in Figure 4.6 which permits the pulsed measurement of I_D, V_{DS} and r_{ds}. This arrangement is adaptable to both p and n channel JFETs with a simple changeover switch.

The scheme incorporates the following basic circuits :

i) Chopped d-c biasing circuit,

ii) A summer for the small signal a-c and the drain bias voltage with a current booster,

iii) A chopped voltage source for measuring the pulsed bias current,

iv) Injection of a small signal a-c voltage for measurement of the a-c small signal drain current,

v) A gate used to chop synchronously the signal fed to the oscilloscope and

vi) A driver for the synchronous shunt switches used for pulsed biasing.

The driving pulse is obtained from a programmable pulse generator and its pretrigger output is used to synchronise the oscilloscope and to generate a gate signal for a synchronous chopping of the signal fed to the oscilloscope. The oscilloscope, Tektronix model 547, is

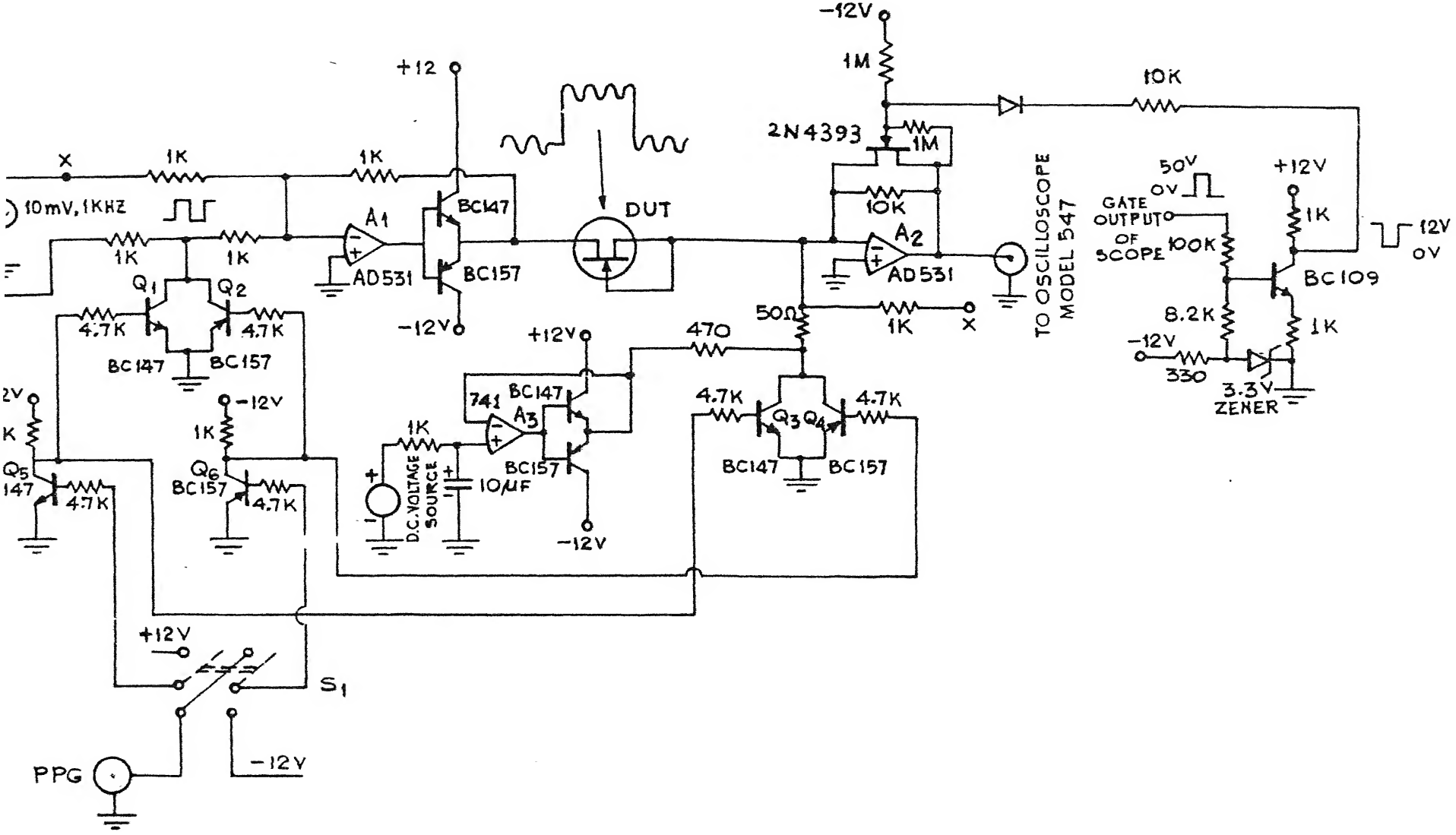


FIGURE-4.6 CIRCUIT DIAGRAM FOR PULSED MEASUREMENT OF I_D, V_{DS} AND r_{ds}

used as a null detector. The synchronous chopper uses the opamp A_2. The pulse driver uses the transistors Q_5 and Q_6 and the drain bias voltage is chopped with the shunt switch using transistors Q_1 and Q_2. The d-c drain current measurement circuit uses transistors Q_3 and Q_4 as a shunt switch and a variable d-c voltage is fed with a proper polarity at the input of the current booster with opamp A_3. The opamp A_1 sums the chopped bias and the small signal voltage and feeds through a current booster to the drain terminal of the device under test. The small signal a-c current through the device is measured by the injection of the same a-c small signal voltage at the input of opamp A_2 through a calibrated attenuator. In order to obtain a base line in the oscilloscope display, the synchronous chopping is necessary so that the small signal a-c voltage component sitting in the space between two successive pulses does not overload the vertical input of the oscilloscope. It is interesting to note that this setup is also adaptable for continuous measurements when the pulse generator is replaced by a d-c voltage source of appropriate polarity.

The experimental plots for a typical sample at five different temperatures are shown in Figure 4.7(a). It may be noted that while the plot is indeed a straight line for $V_{DS} \leq 2V_p$ at each temperature, the variation of the intercept with temperature is much more than the

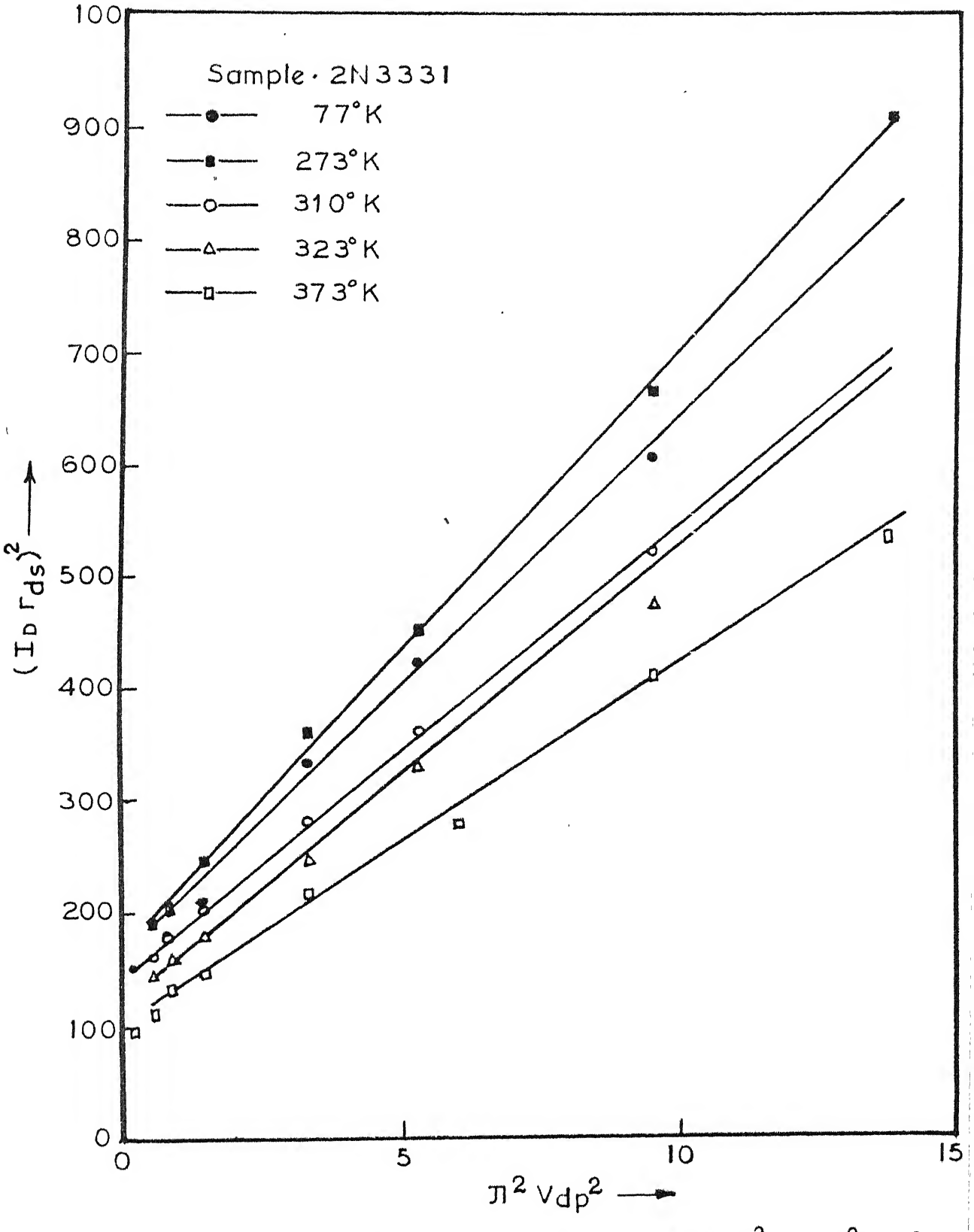


FIGURE-4.7(a) PLOT OF $(I_D r_{ds})^2$ Vs. $\Pi^2 V_{dp}^2$

expected variation of E_o^2.

The computed values of r_{ds} according to the equation (4.24) given by Grebene and Gandhi and (4.25) are shown in Figure 4.7(b) with different applied bias voltages. The experimentally measured points are also plotted for comparison. From the plot, it is quite clear that equation (4.24) holds for small values of the voltages in excess of pinchoff whereas equation (4.25) is valid over a large range of applied bias. This also conforms to the nature of variation of $I_D\ r_{ds}$ as obtained from Grebene-Gandhi model.

4.4.2. Measurement of g_m

Pulsed measurement of g_m is accomplished with a minor alteration of the setup shown in Figure 4.6. The d-c small signal is removed from the input of the opamp A_1. The gate is connected to a d-c bias and a superimposed small signal voltage with respect to the ground (the source being connected to the virtual ground of the opamp A_2). The rest of the scheme is as before.

This measurement has not been pursued due to the contradictions within the model for g_m.

4.4.3. Measurement of c_{gs} and c_{gd}

Pulsed measurement of c_{gs} and c_{gd} are difficult,

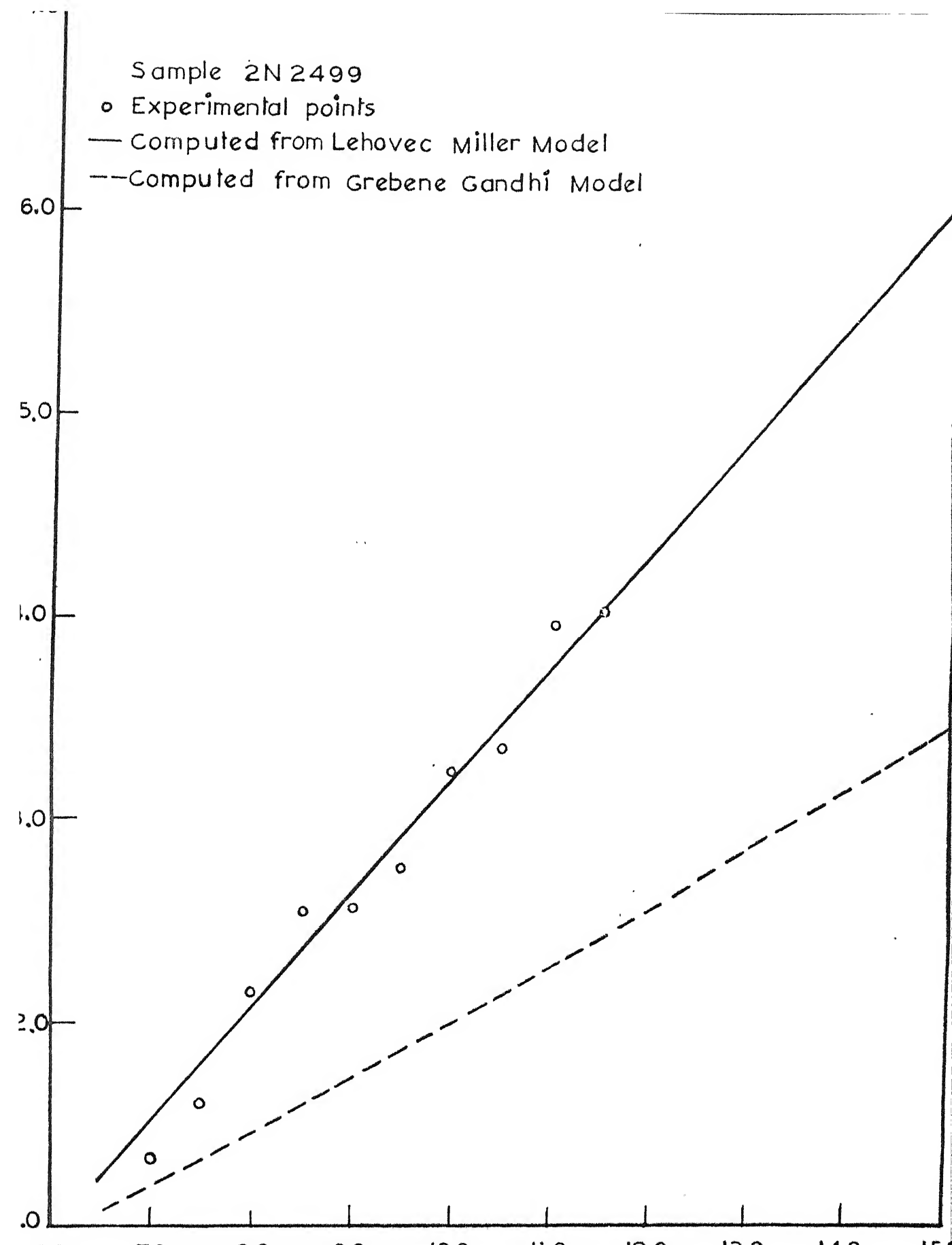


FIGURE-47(b) PLOT OF r_{ds} Vs V_{DS}

hence only continuous bias measurements are carried out. It may be mentioned that this measurement requires a capacitance bridge with a provision for a guard terminal. Boonton capacitance bridge model 74C has the facility of three terminal measurements and has been utilised for the purpose. Biasing of the device has been achieved through the use of an adjustable current source with a very high output impedance. The experimental data has been plotted in Figure 4.5.

4.4.4. Measurement of c_{ds}

Measurement of c_{ds} is rather difficult even under continuous bias due to the following reasons.

i) The magnitude of this capacitance is quite small compared to the other capacitances viz. c_{gs} and c_{gd}. Otherwise, the cutoff frequency in the common source configuration of JFETs would have been decided by this capacitance.

ii) Measurement of such a low capacitance in an active device like JFET is not even possible through a direct replacement type of measurement using standard variable air capacitor in a resonance type circuit due to the presence of the guard terminal in the standard capacitor. The scheme suggested by Misra and Prasad uses this resonance technique with direct substitution at a

frequency as low as 200 khz. which therefore, is questionable.

iii) A direct bridge measurement of this circuit parameter is also not easy due to chances of oscillation and instability in the measurement of y_{12} under common gate configuration at the chosen frequency where the accuracy and the resolution of the measurement is somewhat reasonable. The alternative process of a two step measurement with a commercial VHF admittance bridge e.g. Wayne-Kerr model B 801 is also not meaningful in the sense that the value of c_{ds} obtained as the difference of the measurements of c_{oss} and c_{rss} under the same biasing conditions, incurs appreciable error due to the systematic error of $\pm$ 2.5 pf along with a resolution of 0.5 pf of the instrument.

The technique adopted for this measurement requires a voltmeter with a very low input capacitance e.g. HP model 8405A vector voltmeter, and a neutralised amplifier where the device under test is the only active component. The set up is shown in Figure 4.8. The output amplified voltage is measured with the help of this voltmeter. The neutralisation cancels the feedback effect of c_{gd} and the residual resistive feedback factor is very small. Under such conditions the input and the output ports of the common source amplifier are practically decoupled. Now, the frequency response of the amplifier, neutralised

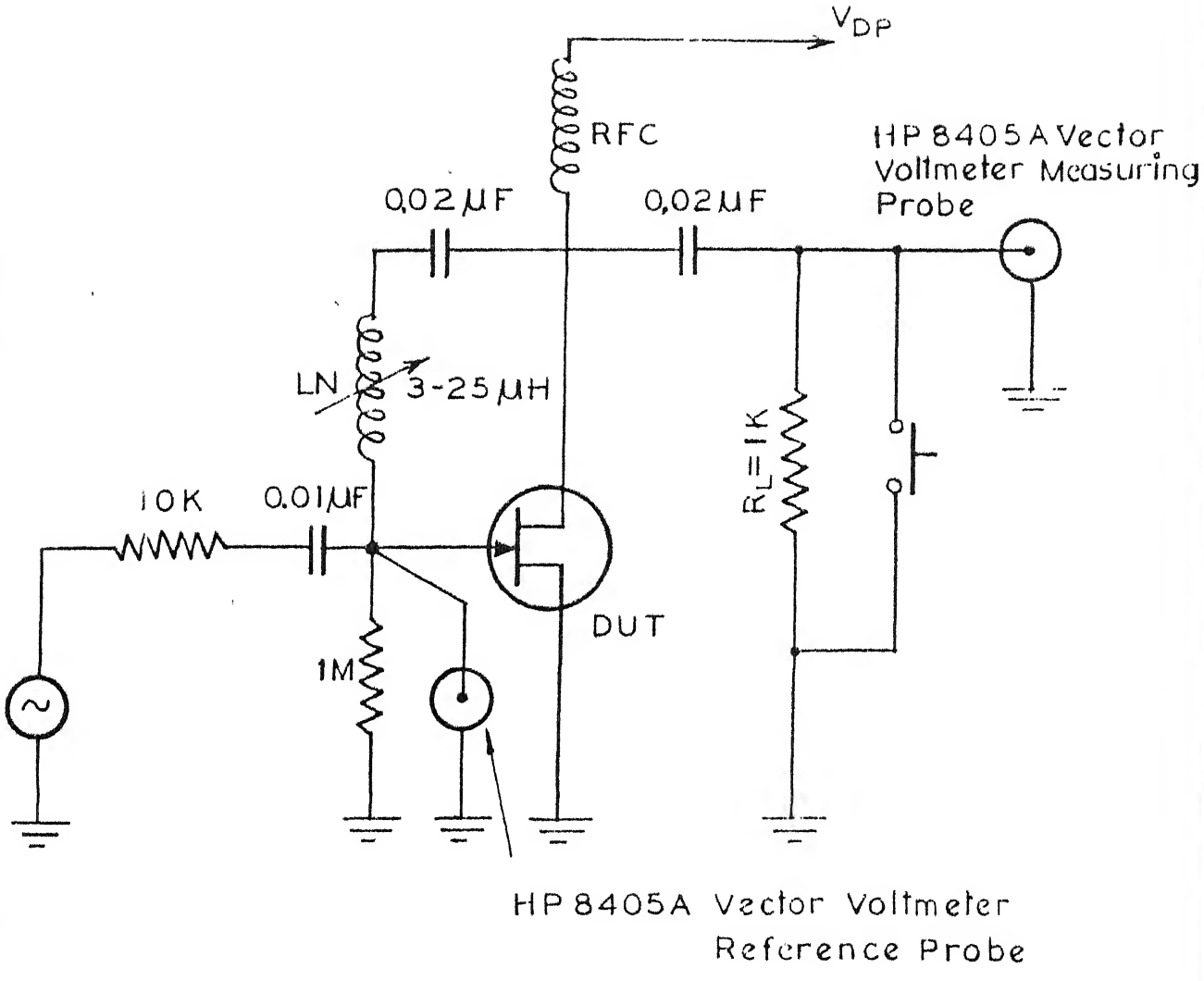


FIGURE-4.8 SETUP FOR MEASUREMENT OF C_{ds}

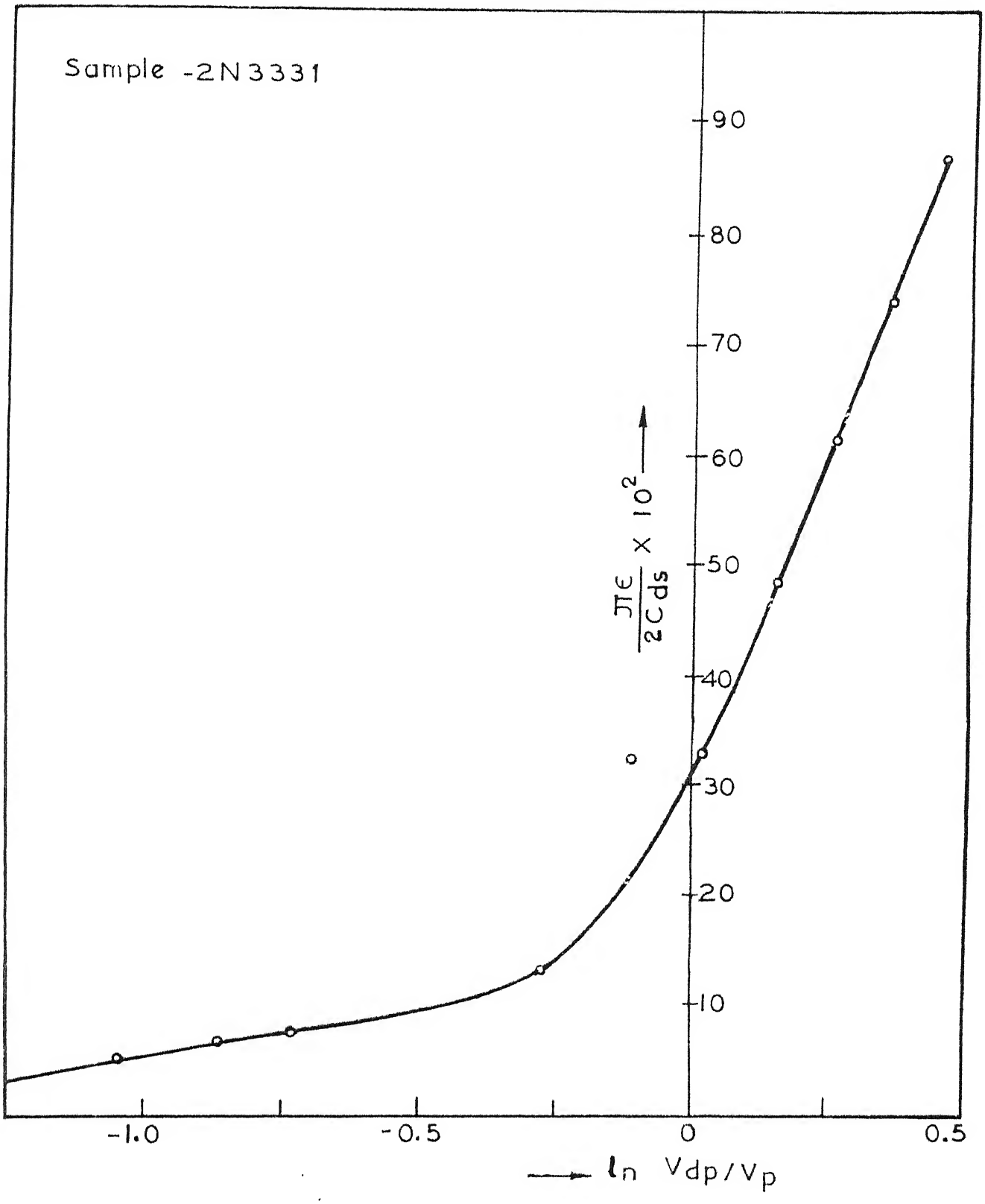


FIGURE- 4.9 $\pi\epsilon/2C_{ds}$ Vs. in Vdp/Vp

a faithful determination of the device parameter relationship from its measurement. Therefore, this circuit parameter is left out for further consideration due to lack of reliable expressions.

The drain-source capacitance c_{ds} is deleted from the list of post-pinchoff circuit parameters as the model is not reliable and the scheme of measurement, although quite sophisticated is not accurate enough for the present purpose.

The expression for c_{gd} as given by equation (4.31) involves a number of auxilliary parameters e.g. x_1, k etc. and is not very much suitable for the present purpose of determination of device parameter relationships from terminal measurement. So, this circuit parameter also is not included for further consideration.

The remaining post-pinchoff circuit parameters of the device are listed below along with the relationship among the device parameters obtained from their measurements.

i) $\frac{L}{a}$, $L\bar{E}_o$ from $I_D\, r_{ds}$

ii) $V_p + V_{bi}$, $\frac{L^2 g_o^2}{12\, \mu_o}$ from c_{gs}

The actual procedure for utilising these relationships has been taken up in chapter 5.

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CHAPTER - V

DETERMINATION OF DEVICE PARAMETERS

The objective of the present work, as outlined in Chapter 1 is to find out a method for determination of the device parameters of a JFET from the measurement of its circuit parameters. The terminal characteristics of a JFET in the parallel-channel, gradual-channel and post-pinchoff regions of operation have been investigated in Chapters2, 3 and 4 respectively, leading to the definition of various circuit parameters. The number of circuit parameters thus defined is more than the number of device parameters. The remaining problem, then is to identify a minimal set of circuit parameters from the possible 'adequate' sets which are sufficient for obtaining a unique solution of the device parameters. The necessary methodology is developed in the next section, followed by the actual evaluation of the device parameters from terminal measurements.

5.1. A methodology

One has to start by considering the expressions for various circuit parameters in the parallel-channel, gradual-channel and post-pinchoff regions of operations as summarised in Figure 5.1. It may be observed that the

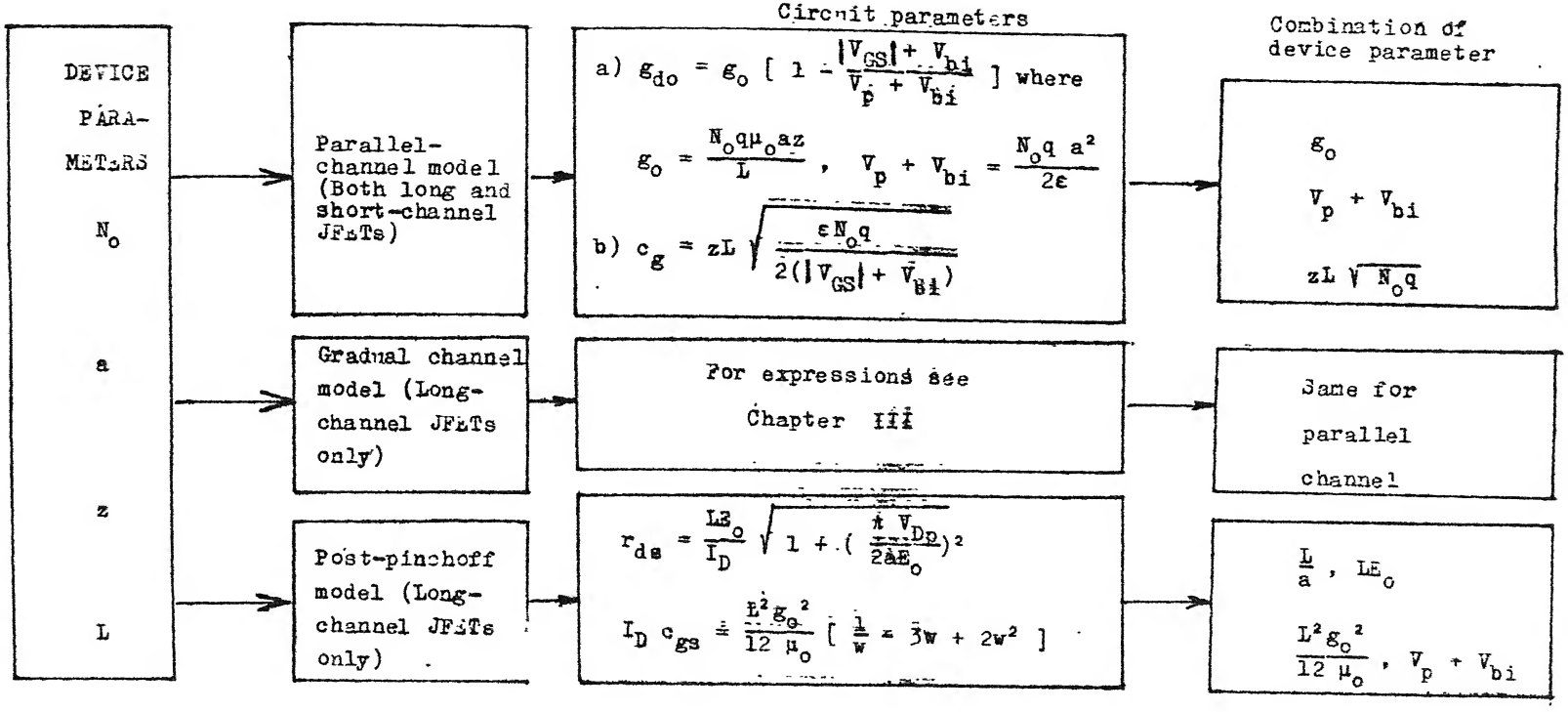


Figure 5.1 Models and the parameter relationships.

measured circuit parameters are related to the bias voltages through algebraic expressions involving the device parameters (N_o, a, z and L) and a few intermediate parameters (g_o, V_p, V_{bi}, μ_o and E_o) which are functions of the device parameters. The values of the intermediate parameters as well as some of the device parameters can be conveniently determined, as already pointed out in earlier chapters, from appropriate plots of the measured circuit parameters against bias voltages. Certain combinations of the device parameters, are directly obtained in this manner from the measurement of a single circuit parameter and are listed in the last column of Figure 5.1.

The primary question to be answered now is whether the device parameters can be uniquely determined from any one of the three models of JFET. As indicated in Figure 5.1, the parallel-channel model is capable of providing values for three combinations of the device parameters. Thus, one more relationship is necessary.

It has been established in chapter 3 that the gradual-channel provides the same information regarding device parameters as obtained from the parallel-channel model whereas the theoretical basis of the gradual-channel model is less reliable. Therefore, for the present purpose the consideration of the gradual-channel model is ruled out and the possibility of its utilisation

will not be directly pursued any further.

The post-pinchoff circuit parameters on the other hand do lead to a clear cut procedure for evaluating the device parameters as shown in the flow chart in Figure 5.2. Therefore, it may be concluded that the device parameters may be evaluated either from the post-pinchoff circuit parameters or from a set of circuit parameters selected from both the parallel-channel and post-pinchoff models. It may be noted that this limitation will not permit the methodology developed here to be applied to short-channel devices which lack any accepted model for gradual-channel and post-pinchoff regions of operation.

The next question is how to select a set of circuit parameters for the solution of the problem. The answer is dependent on two factors :

i) accuracy of the measurement of circuit parameters and

ii) the mutual dependence of the relationships to be used.

A look at Figure 5.1 now reveals that there are altogether four circuit parameters available for measurements in the parallel-channel and post-pinchoff regions of operation of the device.

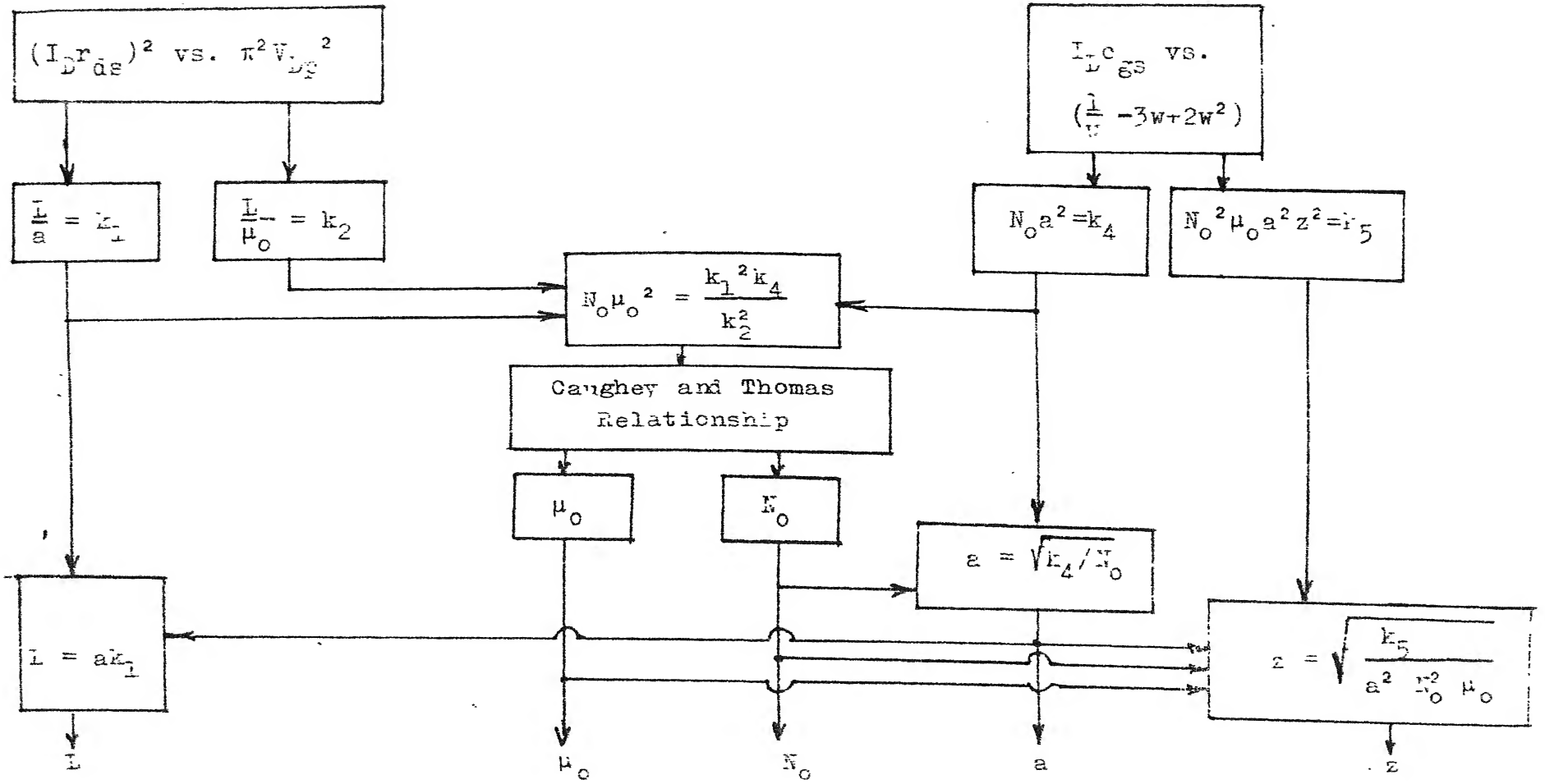


Figure 5.2. Flowchart for evaluation of device parameters from post-pinchoff measurements.

From the measurements of these four circuit parameters one obtains the following combinations of the device parameters :

(i) g_o, (ii) V_p, (iii) $zL\sqrt{N_o q}$, (iv) $\frac{L}{a}$, (v) LE_o and (vi) $\frac{L^2 g_o^2}{\mu_o}$

Of these six, LE_o is excluded because of the unreliability of the intercept in the $(I_D r_{ds})^2$ vs. $(\pi V_{Dp})^2$ plot as mentioned in section 4.4.1. An attempt towards the selection of the possible 'adequate' sets from the remaining five combinations is presented in the following section.

5.2. Selection of the set of circuit parameters

In order to determine the device parameters which are four in number, one would need a minimum of four equations. The previous considerations show that there are five such equations available as given below :

$$\text{i)} \quad \frac{N_o q \mu_o a z}{L} = k_1 \qquad .. \quad (5.1)$$

$$\text{ii)} \quad N_o q a^2 = k_2 \qquad .. \quad (5.2)$$

$$\text{iii)} \quad N_o q (zL)^2 = k_3 \qquad .. \quad (5.3)$$

$$\text{iv)} \quad \frac{L}{a} = k_4 \qquad .. \quad (5.4)$$

$$\text{v)} \quad (N_o q)^2 \mu_o a^2 z^2 = k_5 \qquad .. \quad (5.5)$$

where k_1, k_2, k_3, k_4 and k_5 are the experimentally determined values for the combination of device

parameters shown on left side of the equations (5.1) to (5.5).

Before one can proceed further, it is essential to examine the mutual independence of the set of these five equations. It is easy to show that

$$k_1 \sqrt{k_2 k_3} = k_5 \qquad .. \quad (5.6)$$

From equation (5.6) it is clear that equation (5.4) is independent with respect to the remaining four equations. Therefore, an independent set of equations can be considered with equation (5.4) and any three from the rest. Equation (5.5) is dropped from the set because :

i) This equation is obtained from the circuit parameter c_{gs} in the post-pinchoff region of operation of JFET where the model is less reliable and

ii) the measurement of c_{gs} under pulsed biasing is not accurate and leads to errors.

This leaves four independent equations involving the four device parameters, the corresponding measurements being those of g_o, $V_p + V_{bi}$, c_g and r_{ds}.

Determination of g_o and $V_p + V_{bi}$ can be carried out from the measurements of either g_{do} vs. V_{GS} in the parallel-channel or g_m vs. V_{GS} in the post-pinchoff region of operation of the device. As has been pointed out in chapter 4, the model for g_m is not accurate due

to the number of approximations in the model. Thus one is not sure about the accuracy of the values of g_o and $V_p + V_{bi}$ obtained from this post-pinchoff measurement. Moreover, post-pinchoff measurements require measurements under pulsed biasing condition which is also avoided by this choice. Therefore, measurement of parallel-channel drain conductance g_{do} has been chosen for the determination of these two parameters.

5.3. Method of solution for device parameters

The method of solution using equations (5.1) to (5.4) is given below.

From equations (5.2) and (5.3) one obtains

$$\frac{zL}{a} = \sqrt{\frac{k_3}{k_2}} \qquad .. \quad (5.7)$$

Equations (5.7) and (5.4) directly yield the value of z :

$$z = \sqrt{\frac{k_3}{k_2}} \quad \frac{1}{k_4} \qquad .. \quad (5.8)$$

Substituting the values of z and $\frac{L}{a}$ from equations (5.8) and (5.4) in (5.1) one obtains

$$N_o q \mu_o = k_1 k_4^2 \sqrt{\frac{k_2}{k_3}} \qquad .. \quad (5.9)$$

The product term $N_o q \mu_o$ is thus obtained. The value of N_o is determined by using the empirical relationship of Caughey and Thomas [1]

$$\mu_o = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_o}{N_{ref}}\right)^{\alpha}} \qquad .. \quad (5.10)$$

where the values of μ_{max}, μ_{min}, N_{ref} and α are given in table 5.1.

TABLE 5.1.

Caughey-Thomas relation between N_o and μ_o

Type of impurity	μ_{max} in $cm^2/V\text{-}sec$	μ_{min} in $cm^2/V\text{-}sec$	N_{ref} in atoms/m^3	α
P	495	47.7	6.3×10^{21}	0.72
N	1330	65	8.5×10^{22}	0.76

Utilising equation (5.10) with suitable values picked up from table 5.1, μ_o is substituted in terms of N_o in the expression for $N_o q \mu_o$. N_o is now determined through the solution of the single-variable nonlinear equation. The knowledge of N_o allows 'a' to be obtained from equation (5.2); L is then determined from equation (5.4). Thus all the device parameters are uniquely determined from the measurement of the circuit parameters g_o, $V_p + V_{bi}$, c_g and r_{ds}.

5.4. Experimental results

The experiments have been conducted on commercially packaged JFET devices. The packaged samples are

so chosen as to encompass the entire spectrum of circuit applications using JFETs. The types of sample with their respective areas of applications are presented below :

i) 2N4393 - N channel low resistance analog switch

ii) 2N3331 - P channel analog multiplier and modulator

iii) 2N2498 - P channel general purpose amplifier

iv) 2N3823 - N channel low capacitance UHF amplifier

v) 2N4416 - N channel high conductance UHF amplifier and oscillator

vi) BFW 11 - N channel general purpose amplifier

Before one undertakes the measurement of the selected circuit parameters for each of these JFETs one must ascertain whether the device is long-channel or short-channel. As pointed out in chapter 3, this is conveniently done by means of the Wedlock test. The circuit parameters are measured only for the devices which satisfy gradual channel approximation as indicated by this test. The sequence in which the measurements are done is as follows :

i) g_{do} (which gives the value for V_p and V_{bi} required for the Wedlock test),

ii) Wedlock test

iii) c_g and

iv) r_{ds}, the last two measurements being done only for long-channel JFETs.

5.4.1. g_o, V_p and V_{bi} from measurements of g_{do}

Measurements of open channel conductance g_o and pinchoff voltage V_p have been carried out for the samples as described in chapter 2. The plots of g_{do} vs. V_{GS} are shown in Figure 5.3 (a-f). Table 5.2 presents the values of g_o and $V_p + V_{bi}$ for each of the samples.

TABLE 5.2

$V_p + V_{bi}$ and g_o from measurements of g_{do}

Sample	Pinchoff voltage $V_p + V_{bi}$ in volts	Open channel conductance g_o in mho
2N4393	1.01	18.2×10^{-3}
2N3331	3.95	3.42×10^{-3}
2N2498	3.22	3.6×10^{-3}
2N3823	3.15	7.63×10^{-3}
2N4416	2.55	7.34×10^{-3}
BFW 11	2.98	8.7×10^{-3}

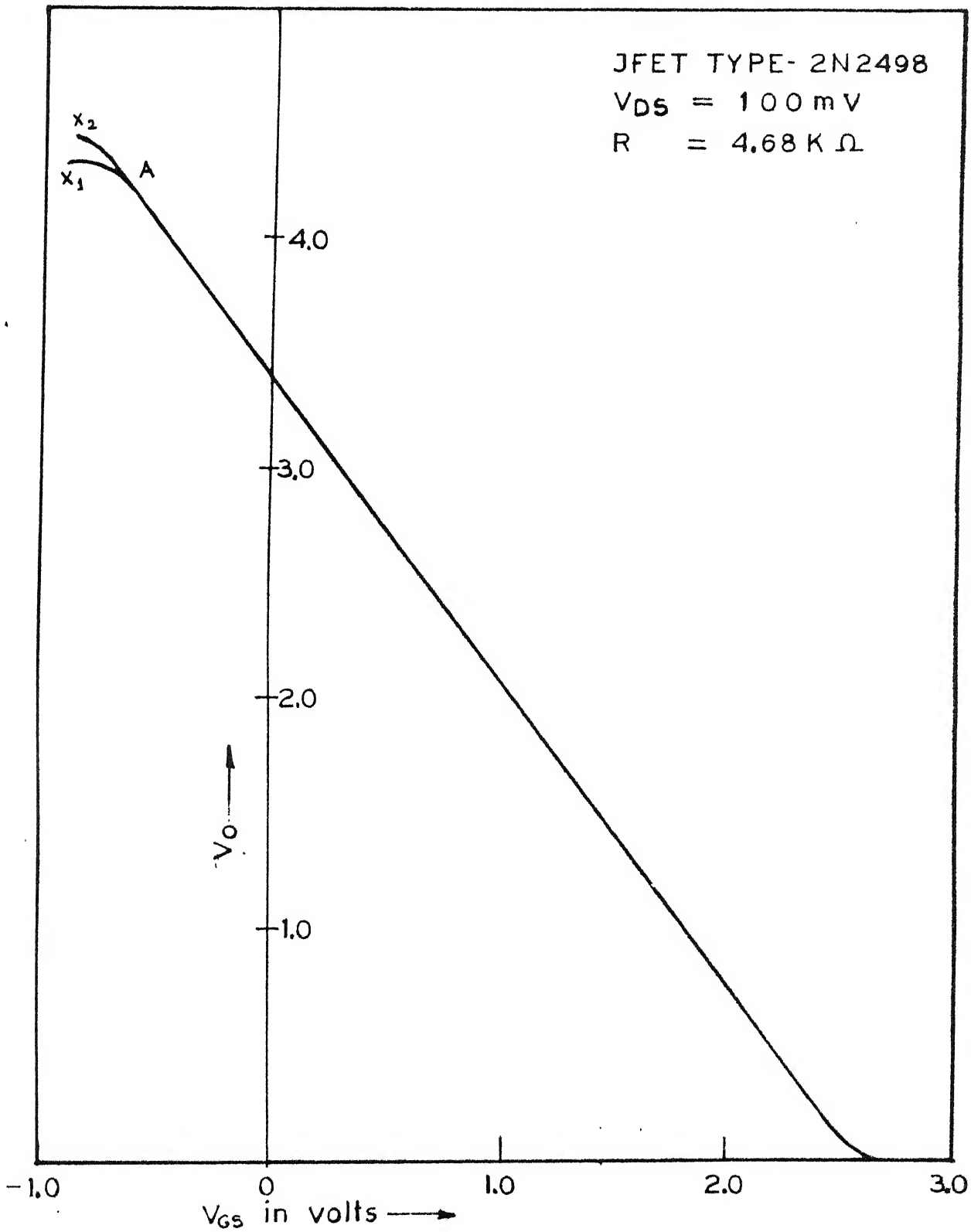


FIGURE- 5.3(C) X-Y PLOT FOR DETERMINATION OF V_P, V_{bi}, G_O.

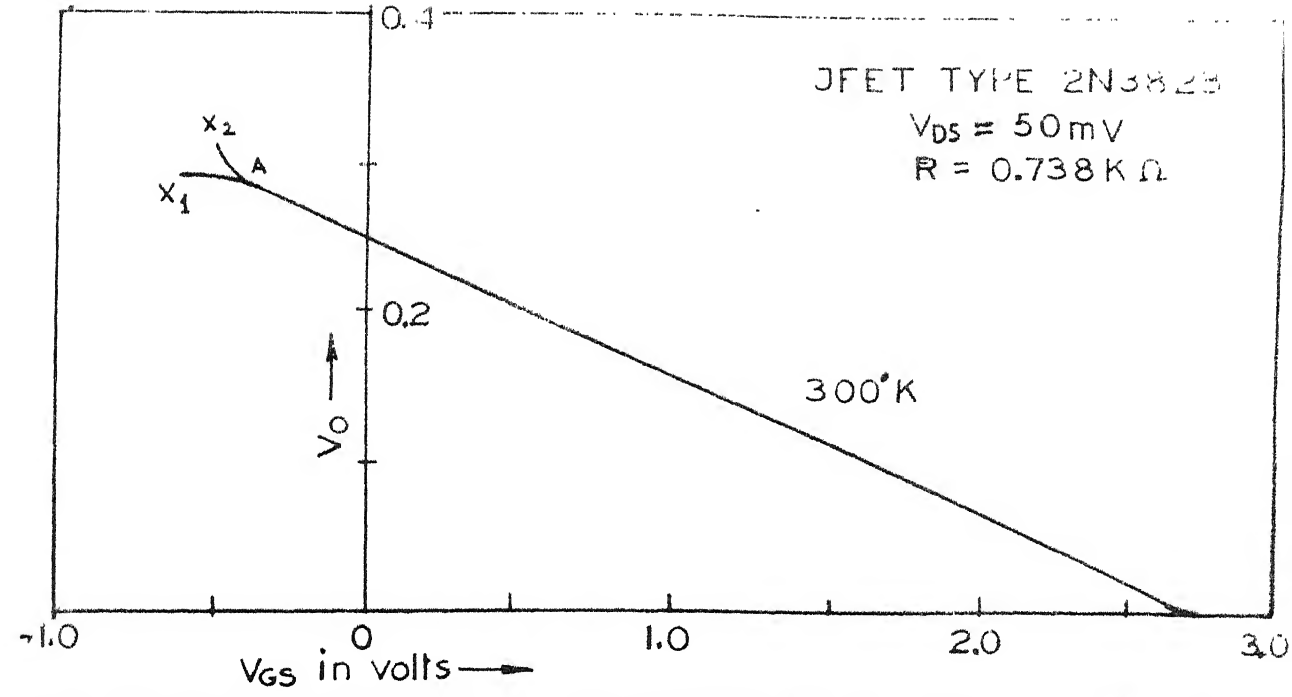


FIGURE- 5.3(d) X - Y PLOT FOR DETERMINATION OF V_p G_o & V_{bi}

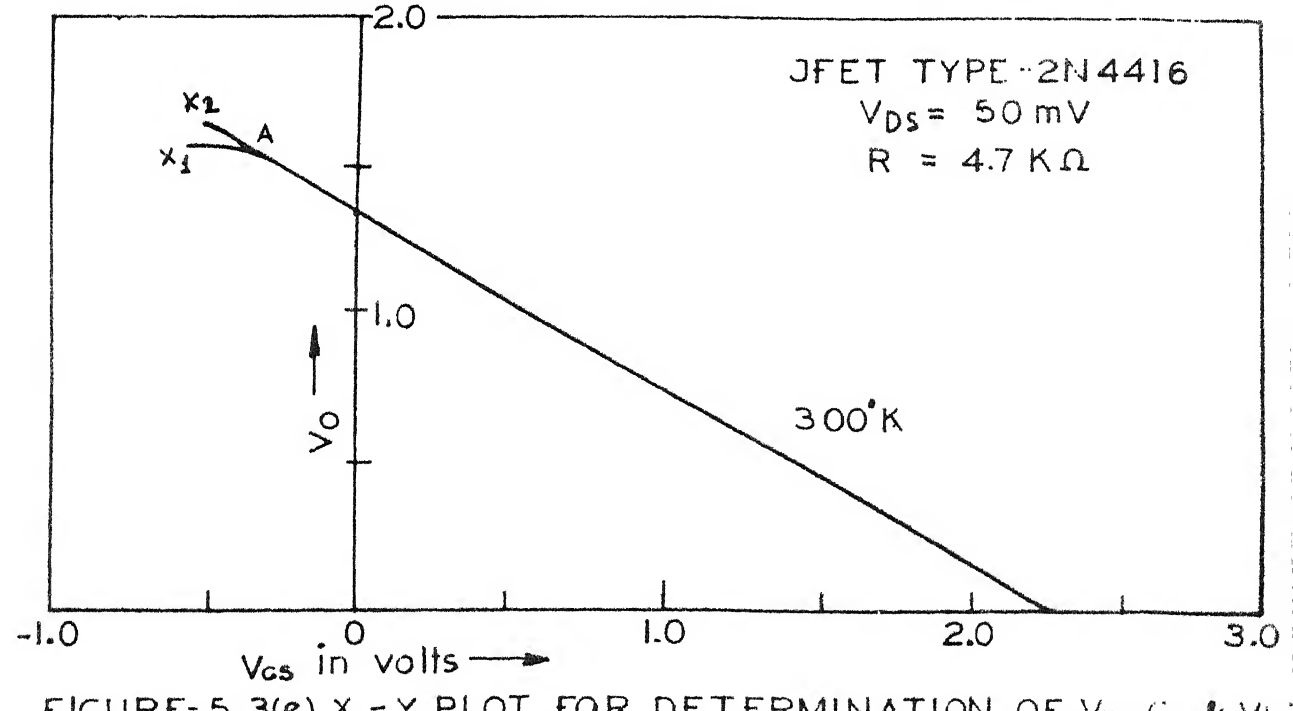
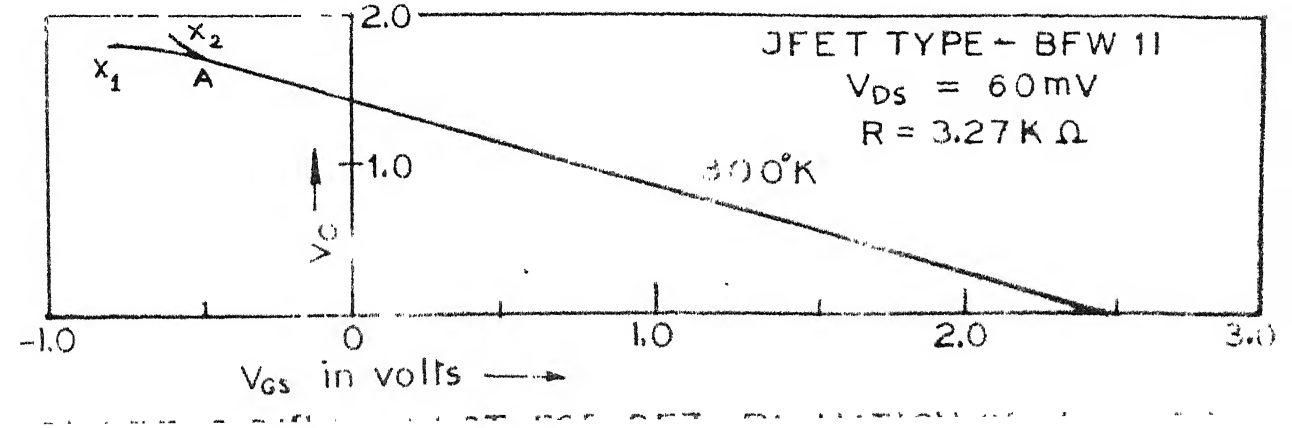


FIGURE- 5.3(e) X - Y PLOT FOR DETERMINATION OF V_p, G_o & V_{bi}



5.4.2. Wedlock test

The plots of I_D vs. V_{DS} characteristics obtained under pulsed biasing in the pre-pinchoff region of operation are presented in Figure 5.4 (a - f); the characteristics of the JFETs 2N4393, 2N2498 and 2N3331 obey the gradual channel approximation whereas the rest do not.

Although pulsed measurements have been done for this test, the experiments with continuous d-c bias have been found to yield identical results.

5.4.3. Measurement of c_g

The measurement of parallel-channel capacitance c_g has been done as discussed in chapter 2. The results are plotted in graphs with $\frac{1}{c_g^2}$ as ordinate and the bias voltage V_{GS} ($0 < |V_{GS}| < V_p$) as the abcissa in Figures 5.5 (a - c) for the samples qualifying the Wedlock test. The plots are nearly straight lines. The results obtained from these plots are presented in table 5.3.

TABLE 5.3

$N_o q(zL)^2$ from measurements of c_g.

Sample	$N_o q(zL)^2$ in coulomb-cm.
2N4393	5.76×10^{-10}
2N3331	6.57×10^{-10}
2N2498	1.56×10^{-10}

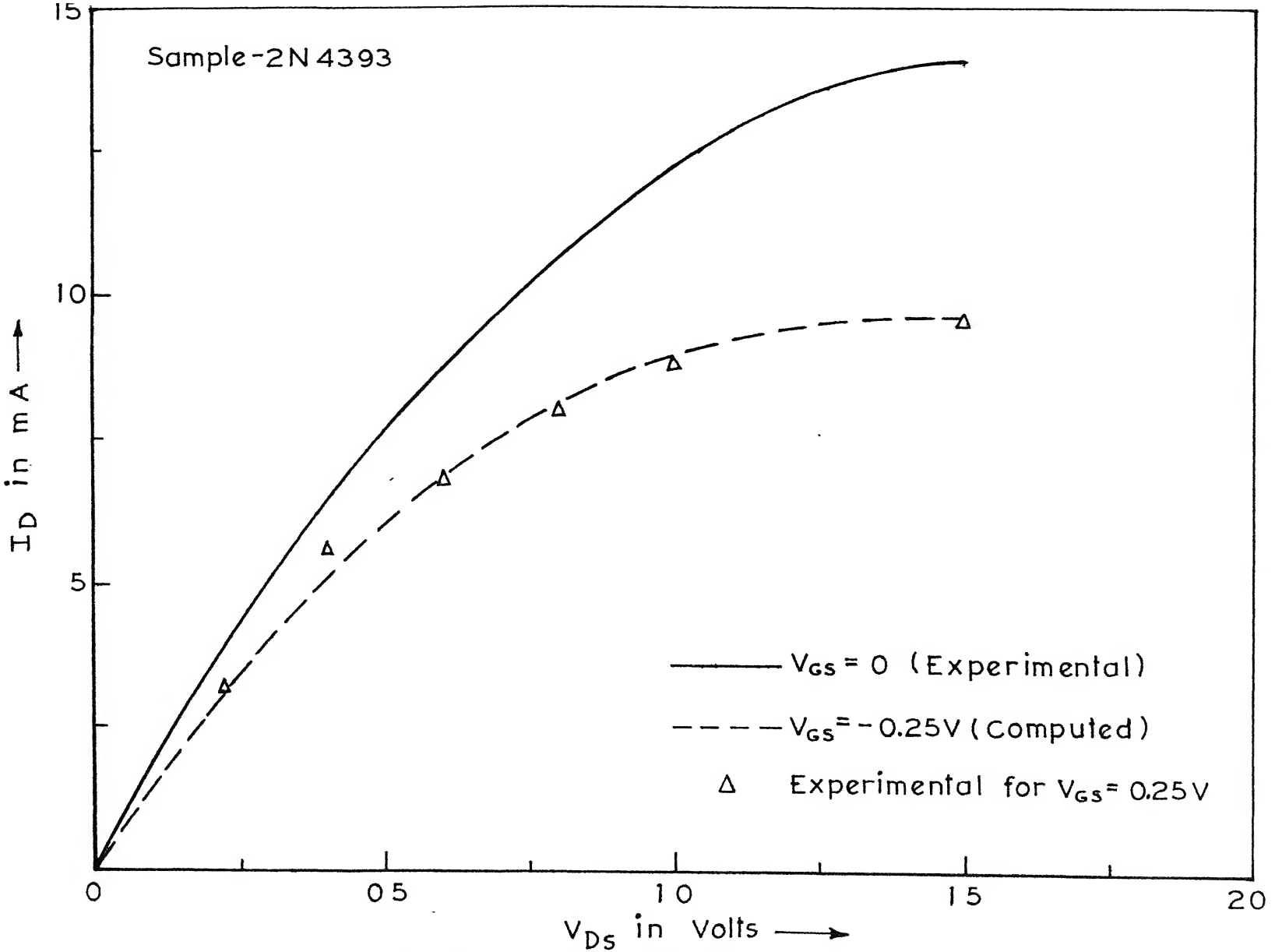


FIGURE- 5.4(a) WEDLOCK TEST

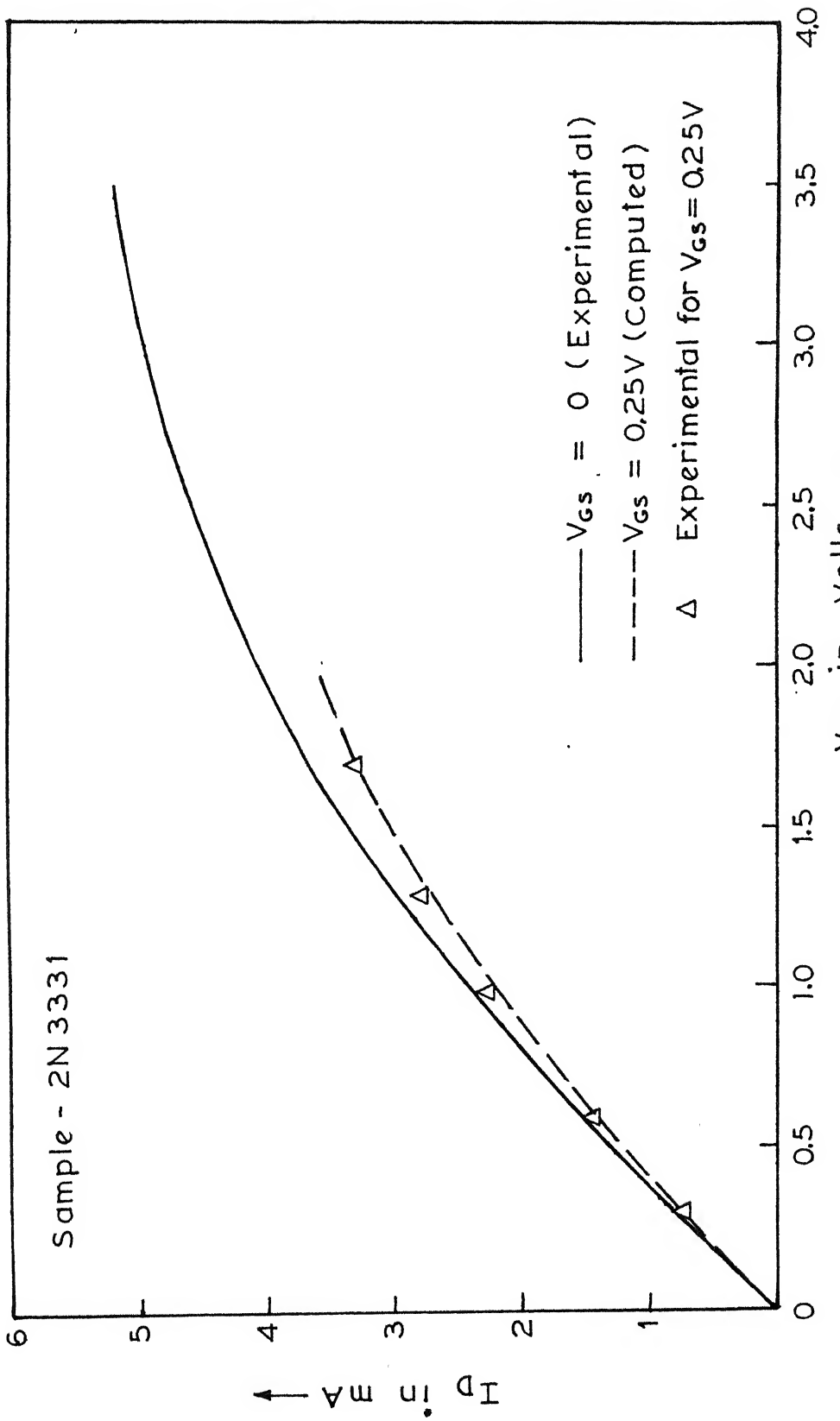


FIGURE - 5.4(b) WEDLOCK TEST

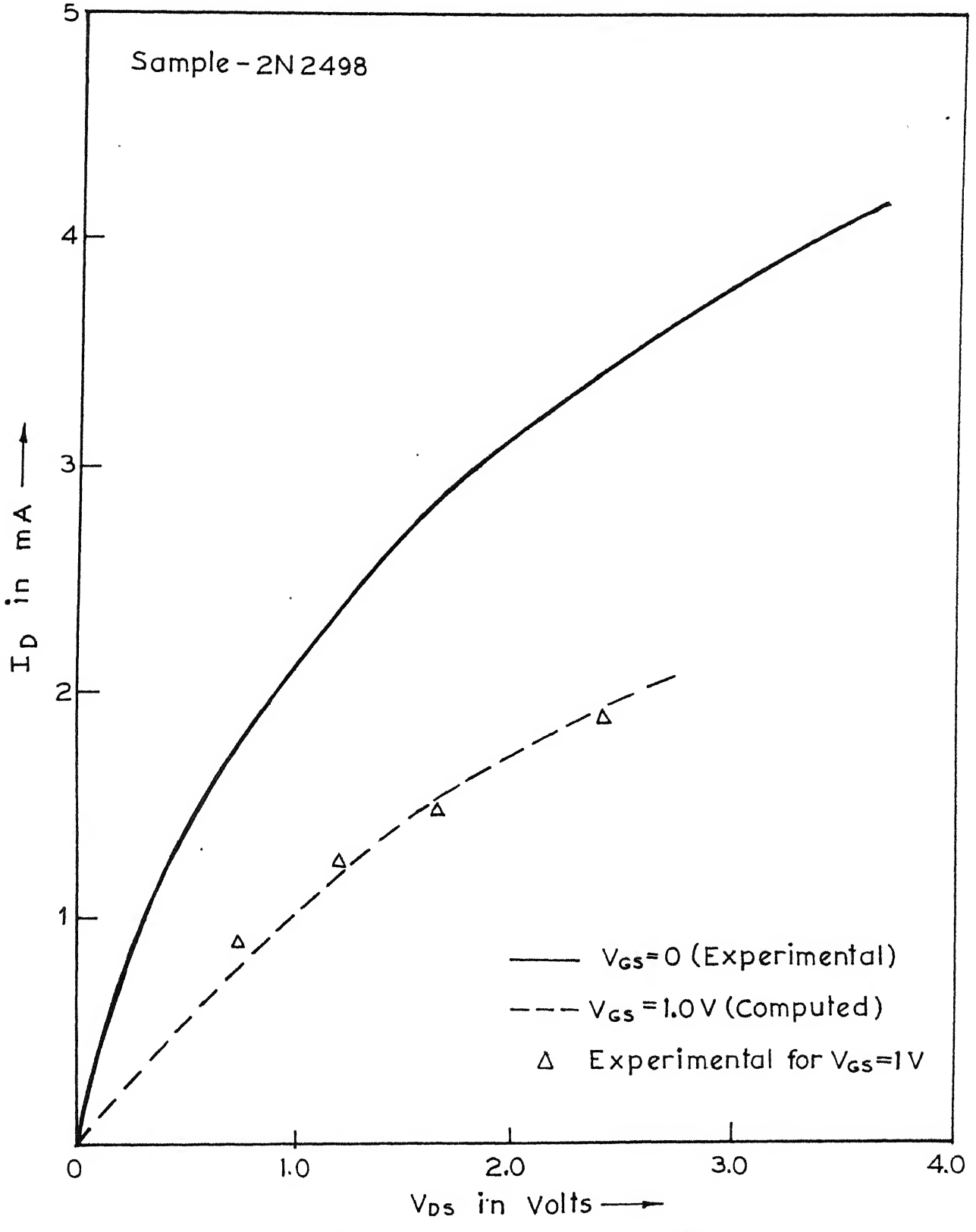


FIGURE- 5.4(c) WEDLOCK TEST

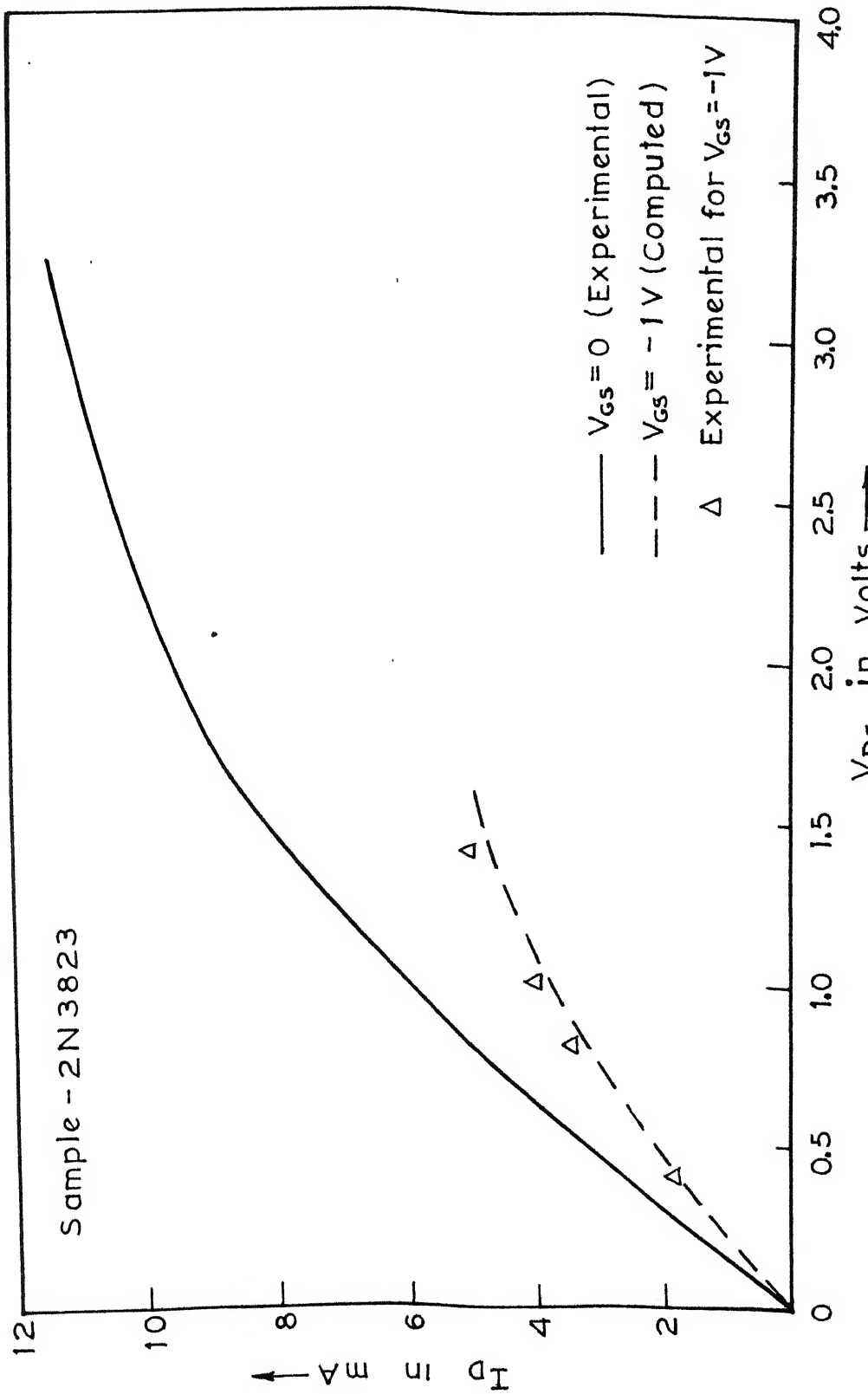


FIGURE - 5.4 (d) WEDLOCK TEST

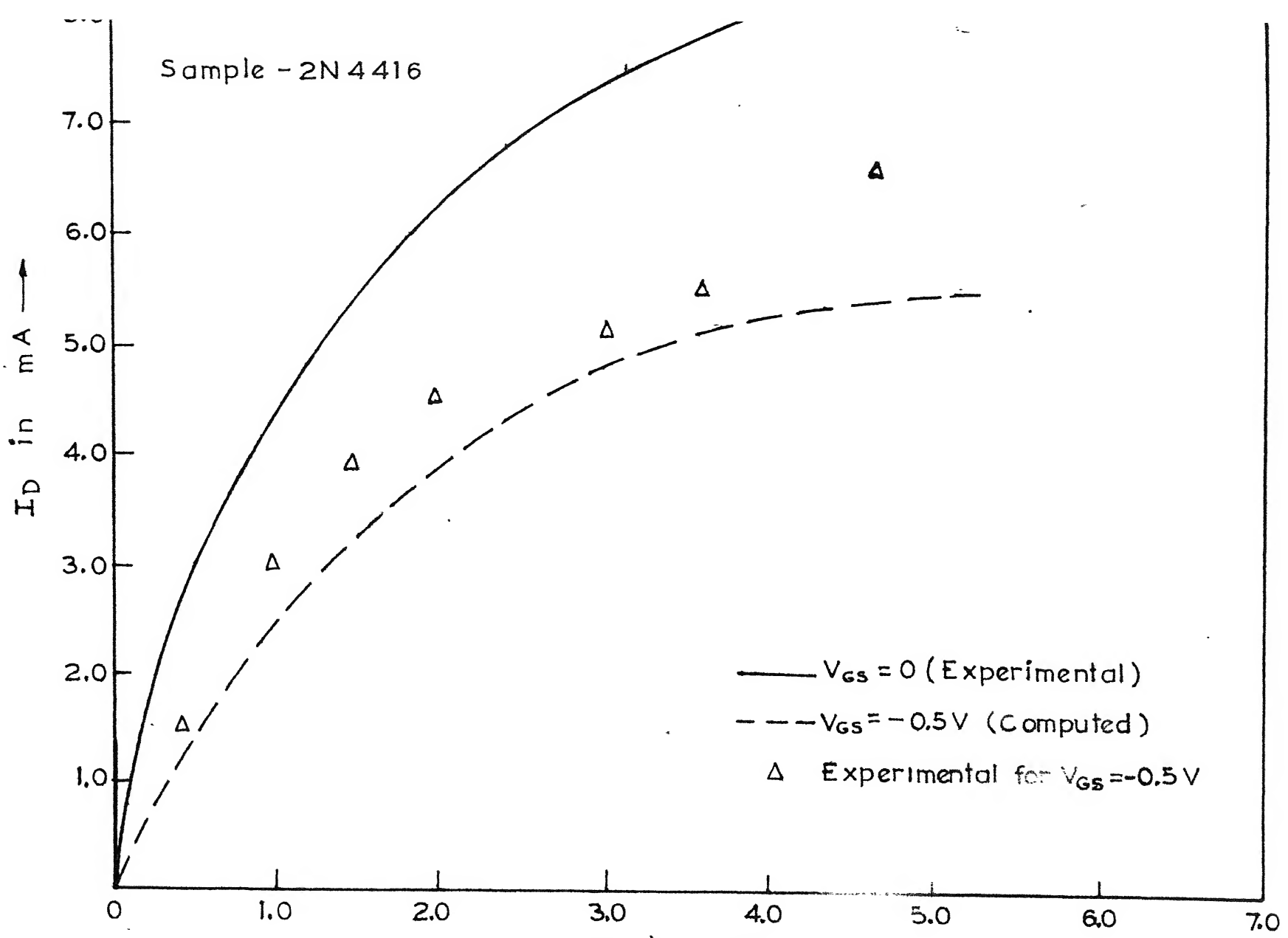


FIGURE - 5.4(e) WEDLOCK TEST

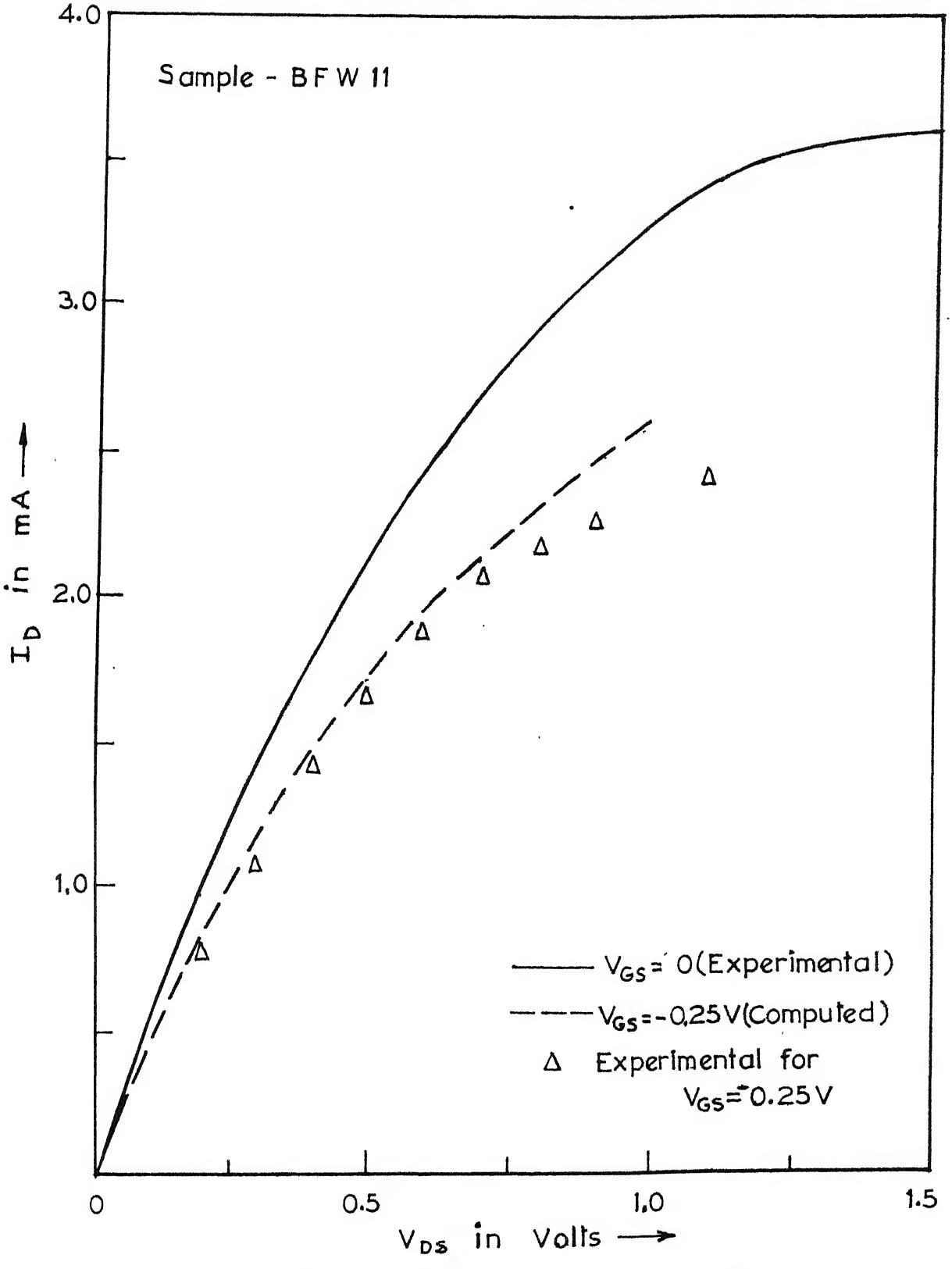


FIGURE - 5.4(f) WELDLOCK TEST

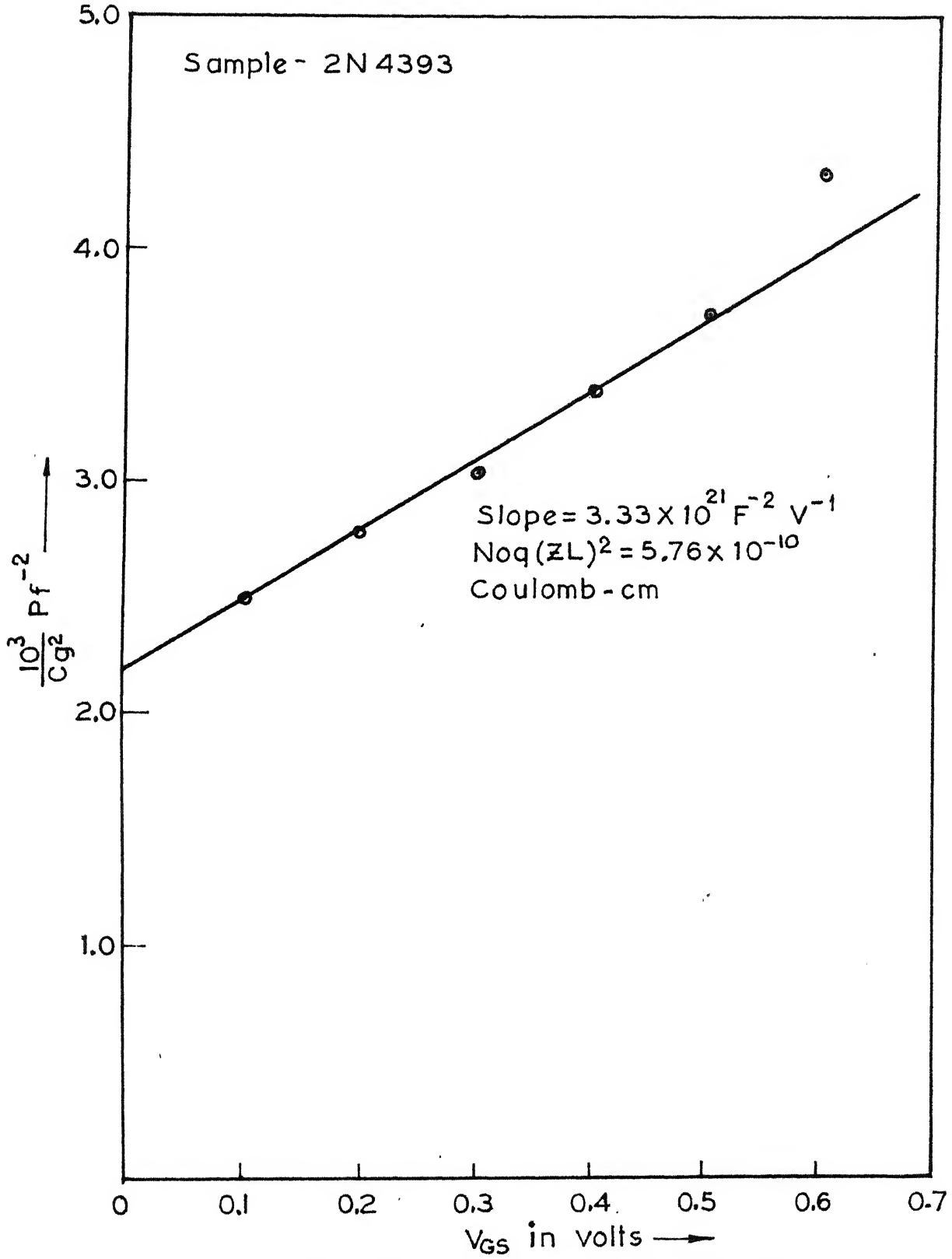


FIGURE - 5.5(a) C - V PLOT

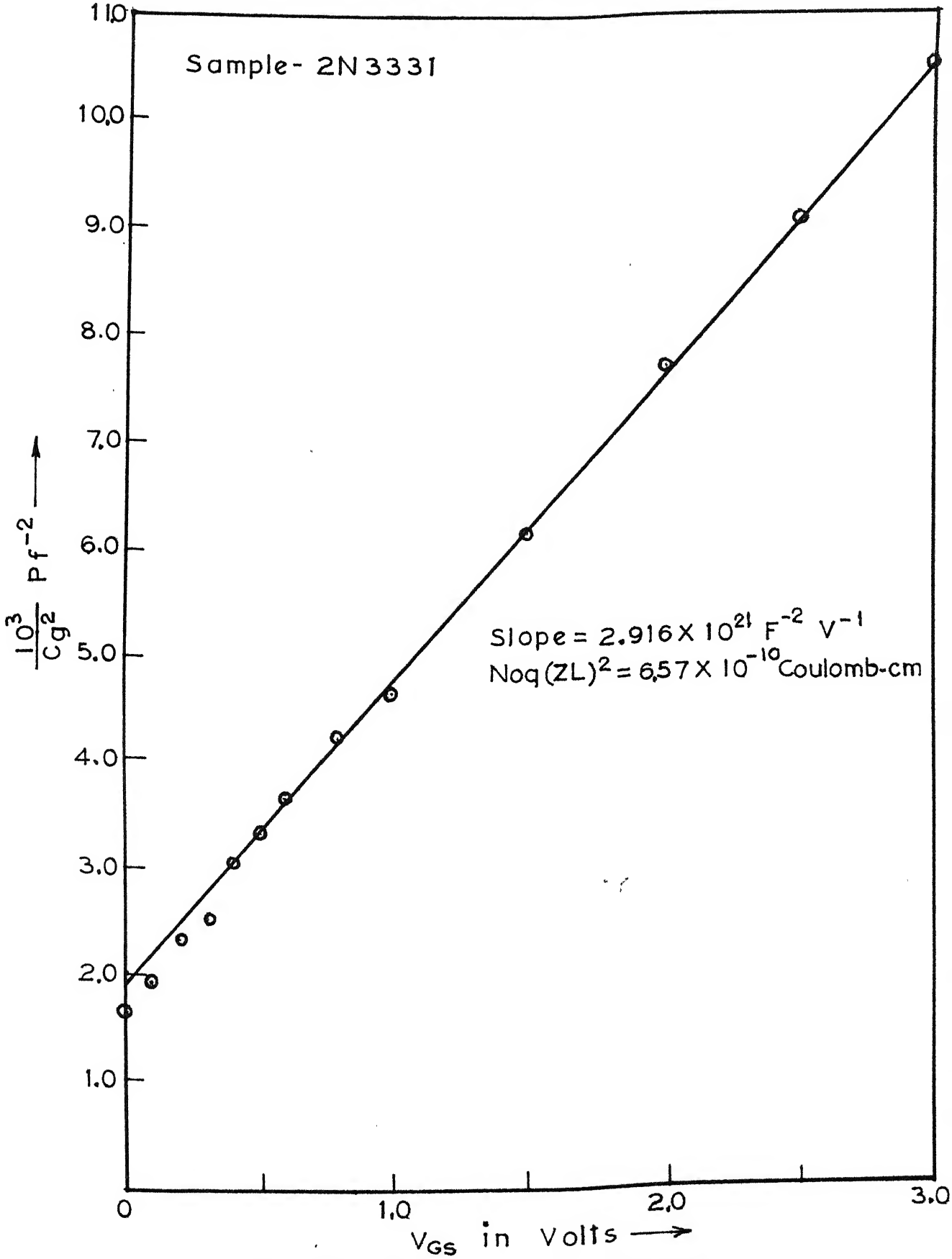


FIGURE- 5.5(b) C - V PLOT

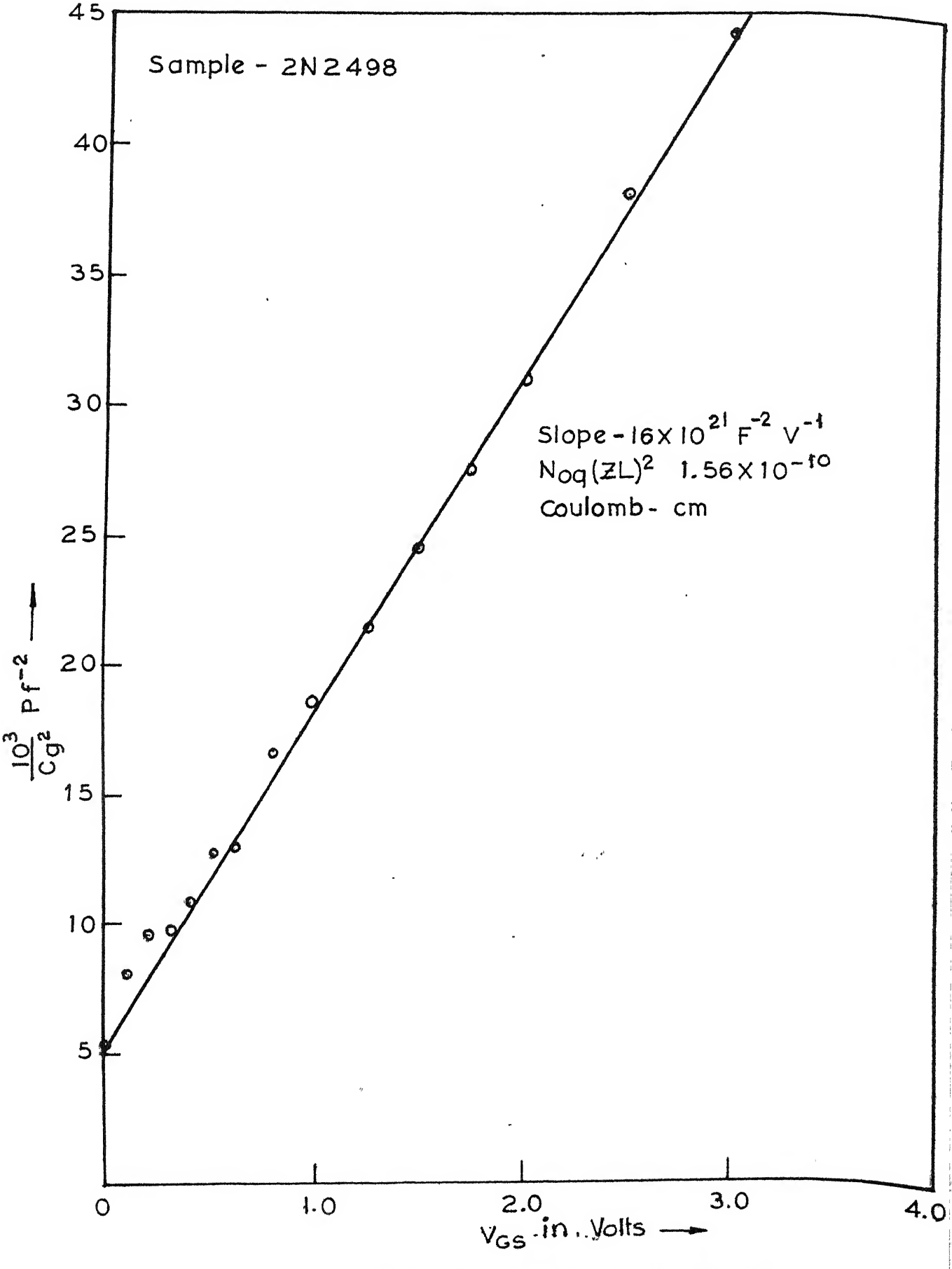


FIGURE - 5.5(c) C - V PLOT

5.4.4. Measurement of r_{ds} in the post-pinchoff region

The results are plotted in Figures 5.6 (a-c) as mentioned in chapter 4. The slope of the characteristics of $(I_D\ r_{ds})^2$ vs. $\pi^2 V_{Dp}{}^2$ gives the value of $\frac{L^2}{4a^2}$ which is independent of channel impurity concentration. The slope of the characteristics is a weak function of temperature whereas the intercept changes appreciably with temperature. The parameter LE_o obtained from the intercept has not been considered due to this reason. The results of the test at room temperature has been presented in table 5.4.

TABLE 5.4

Values of $\frac{L}{a}$ from measurements of r_{ds}

Sample	$\frac{L}{a}$
2N 4393	9.26
2N 3331	10.33
2N 2498	12.0

5.5. Determination of device parameters

The results are tabulated in table 5.5 for the three samples satisfying gradual channel approximation. These dimensions and impurity concentrations are the

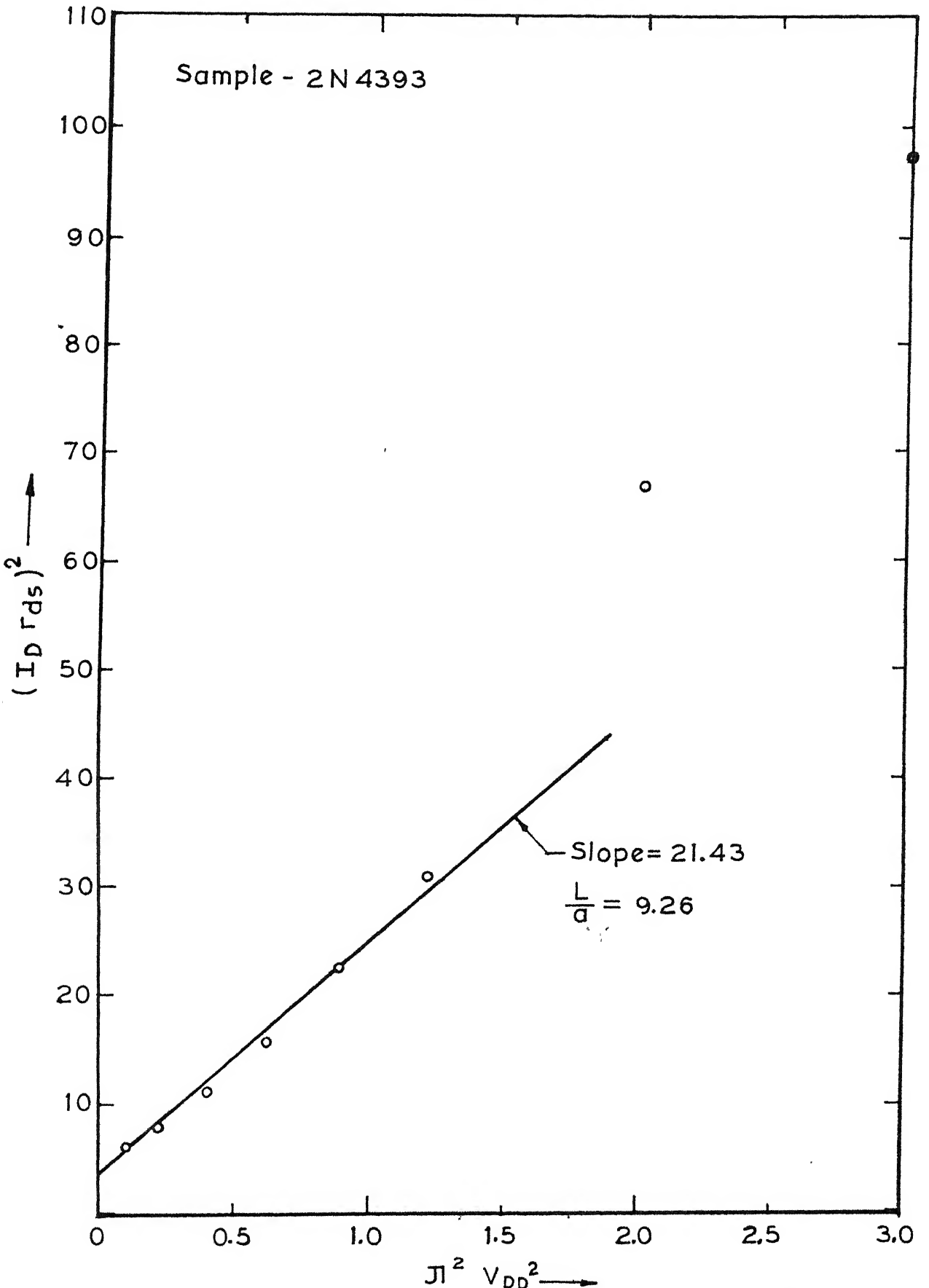


FIGURE- 5.6(a) PLOT OF $(I_D r_{ds})^2$ vs $\pi^2 V_{DP}^2$

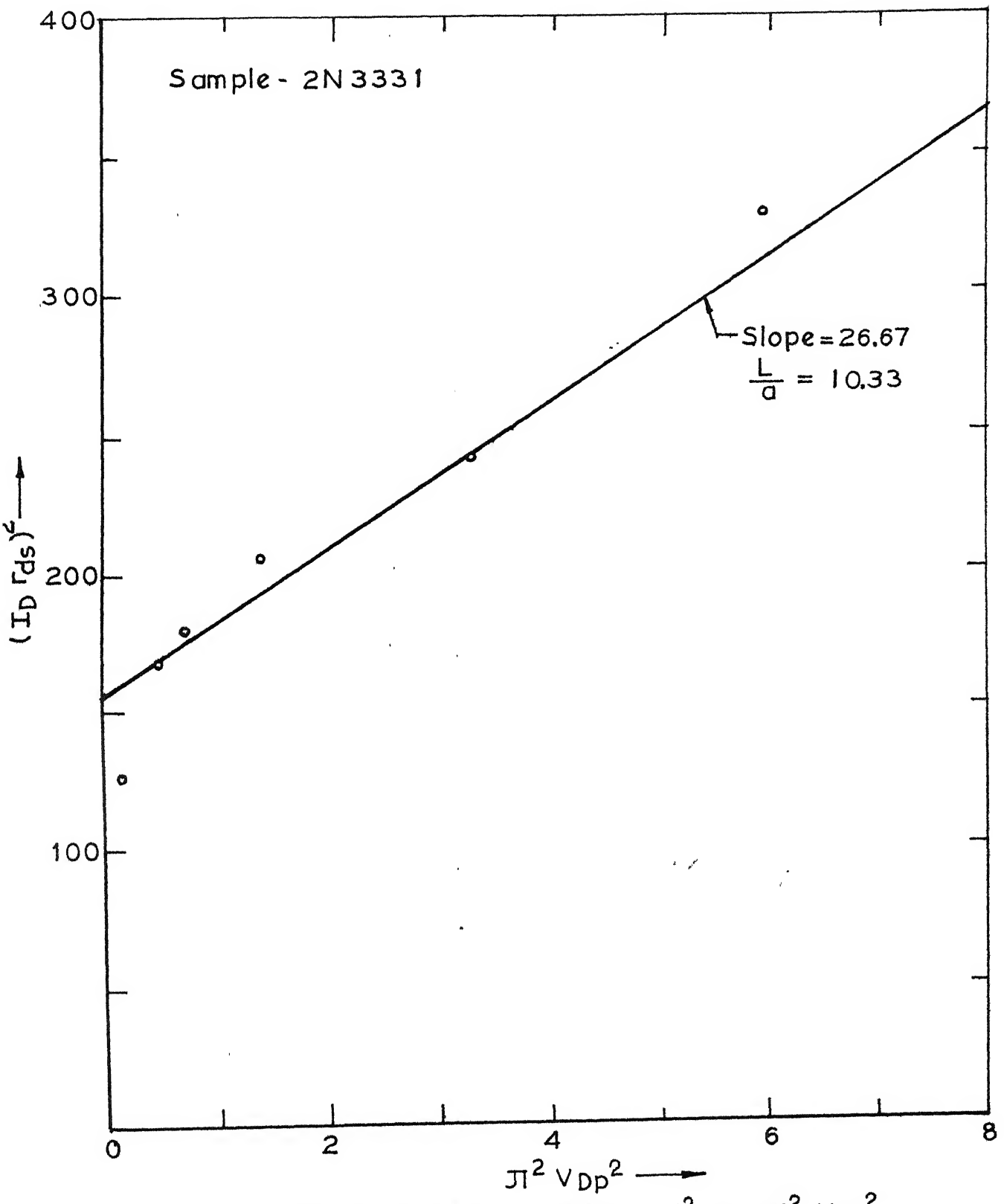


FIGURE - 5.6(b) PLOT OF $(I_D r_{ds})^2$ Vs $\Pi^2 V_{DP}^2$

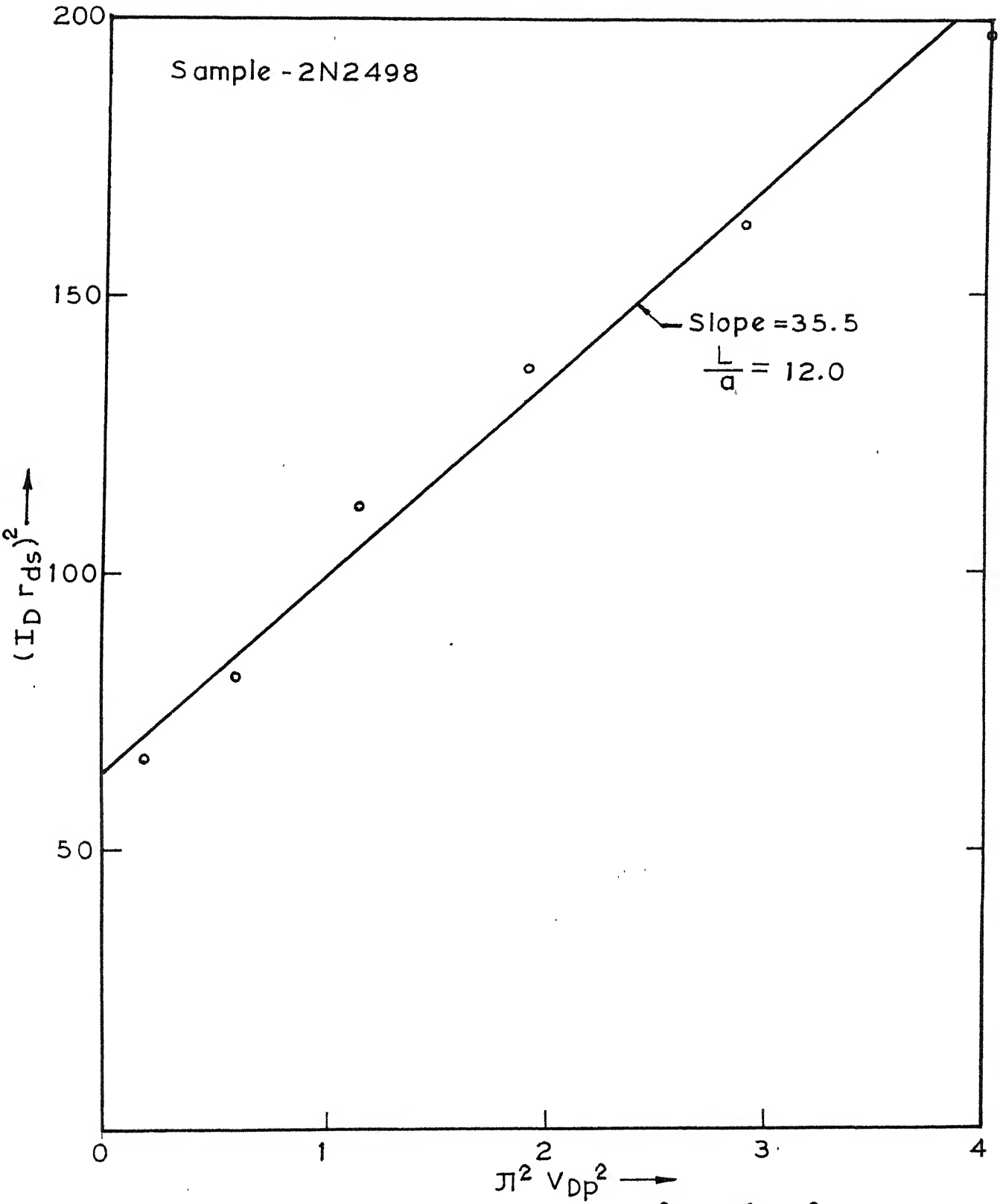


FIGURE - 5.6(C) PLOT OF $(I_D r_{ds})^2$ Vs $\pi^2 V_{DP}^2$

'effective' structural and material parameters of these JFETs. The validity of these parameters are discussed in the following section.

TABLE 5.5

Device parameter values

Sample	N_o in atoms / m^3	a in μm	L in μm	z in mm
2N 4393	4.5×10^{20}	1.71	15.8	17.85
2N 3331	6.0×10^{20}	2.93	30.0	8.64
2N 2498	1.5×10^{21}	1.67	20.0	4.0

5.6. Cross-checks

As has been discussed earlier, the device parameters determined above are 'effective parameters', so the validity of the results has to be established by direct measurement of other circuit parameters which are evaluated from theoretical expressions using the values of the device parameters. The circuit parameters c_{iss} and c_{gs} have been used for this verification. While judging this validity it must be borne in mind that the concept of effective device parameters will always lead to certain percentage of error in calculation of any intermediate parameters or the circuit parameters. This

is accountable to the inherent approximations in the lumped model and the degree of accuracy of the model from which the parameter is calculated.

The circuit parameters which have not been used in the evaluation of the device parameters are the ones to be utilised for the purpose of cross-checking the values of the device parameters. A look into the Figure 5.1 shows that the circuit parameters c_{iss} and c_{gs} are the parameters left unused. In the following subsections the results of the cross-checks with the device parameter combinations obtained from the measurement of c_{iss} and c_{gs} are presented.

5.6.1. Checks with measurements of c_{iss}

It has been pointed out in section 3.2.2. that the parameter c_{iss} may be expressed as

$$\frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} [1 - f(u_1, u_2)] \quad .. \quad (5.11)$$

The form of the equation (5.11)remains unaltered irrespective of the assumptions of either constant mobility or field dependent mobility. For the present case the field dependent mobility has been considered for the function $f(u_1, u_2)$ as

$$f(u_1,u_2) = \frac{3}{4} \frac{(u_1^2 + u_2^2)(u_1 + u_2)}{u_1^2 + u_1 u_2 + u_2^2} \quad .. \quad (5.12)$$

This opinion is primarily due to the fact that the field velocity characteristics is linear over a small range of values of the electric field [2]. The electric field in the residual channel varies over a wide range even in gradual channel operation. This justifies the suitability of the equation (5.12) for the purpose. The lower values of $f(u_1, u_2)$ lead to the operation of the device nearer to drain-current saturation. So the tendency towards violation of the gradual channel approximation is more. For this reason the slope of the characteristic as shown in Figure 3.3 is utilised rather than the intercept on the $\frac{1}{c_{iss}}$ axis. The values of $\frac{zL}{a}$ obtained from the measurements of c_{iss} at different bias are compared with the ones computed from the calculated values of the device parameters. The result is presented in table 5.6 and the plots of equation (5.11) based on measurement are shown in Figures 5.7 (a - c).

TABLE 5.6

Comparison of $\frac{zL}{a}$

Sample	Computed value of $\frac{zL}{a}$	$\frac{zL}{a}$ obtained from c_{iss}
2N 4393	0.165 m	0.165 m
2N 3331	0.0864 m	0.123 m
2N 2498	0.048 m	0.0843 m

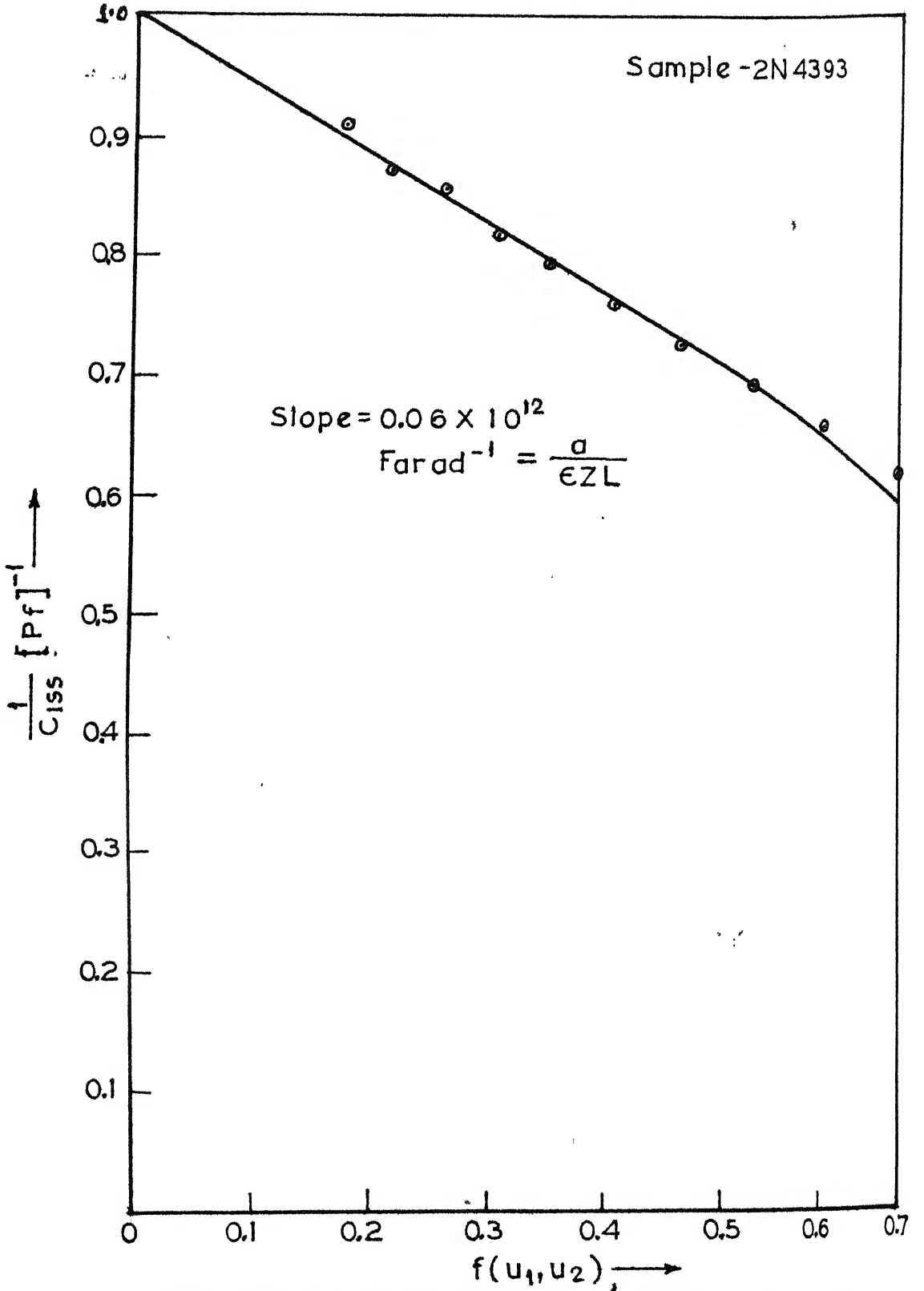


FIGURE- 5.7 (a) PLOT OF $\frac{1}{C_{iss}}$ Vs. $f(u_1, u_2)$

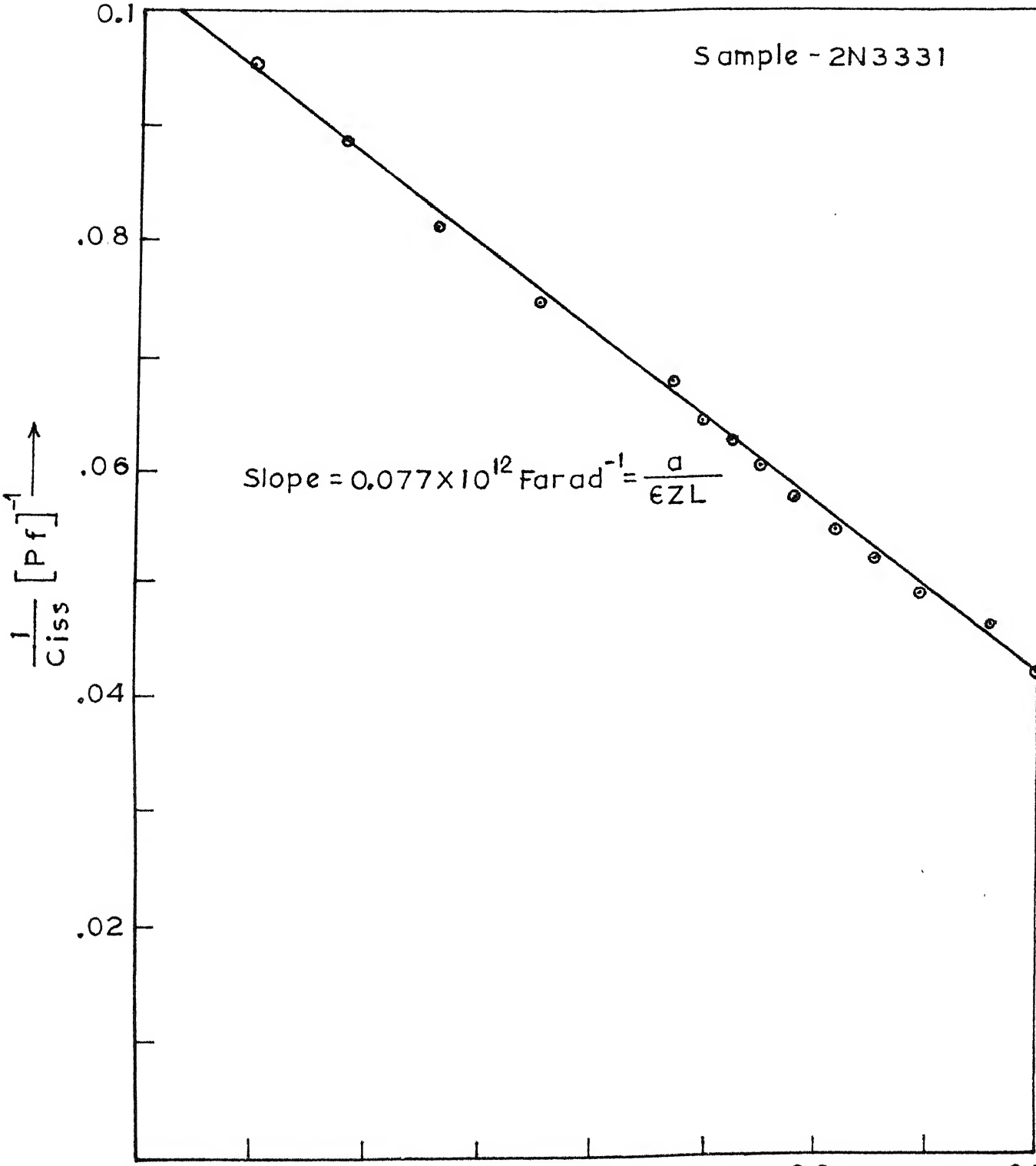


FIGURE- 5.7(b) PLOT OF $\frac{1}{C_{iss}}$ Vs. $f(u_1, u_2)$

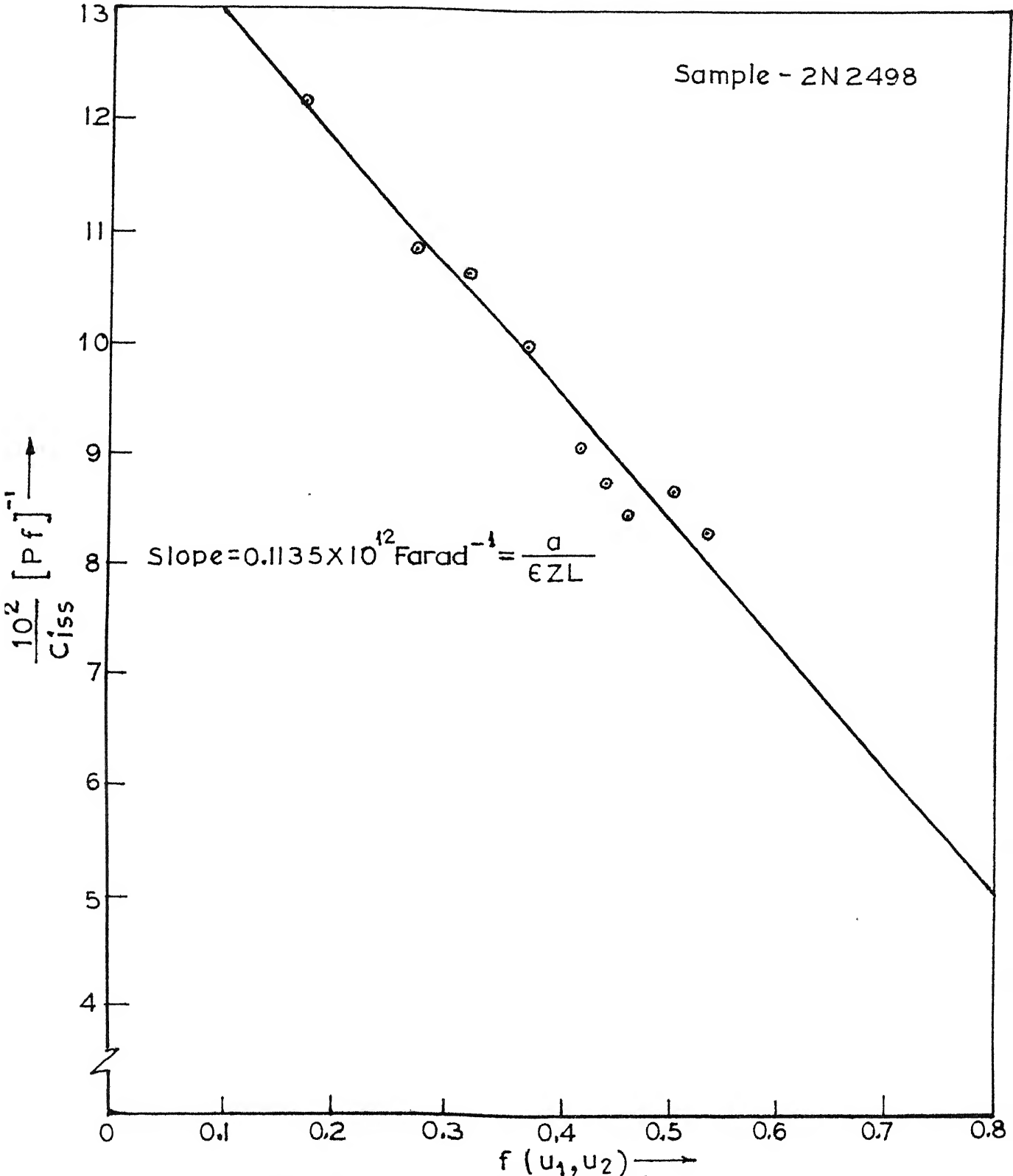


FIGURE- 5.7(C) PLOT OF $\frac{1}{C_{iss}}$ Vs. f (u_1, u_2)

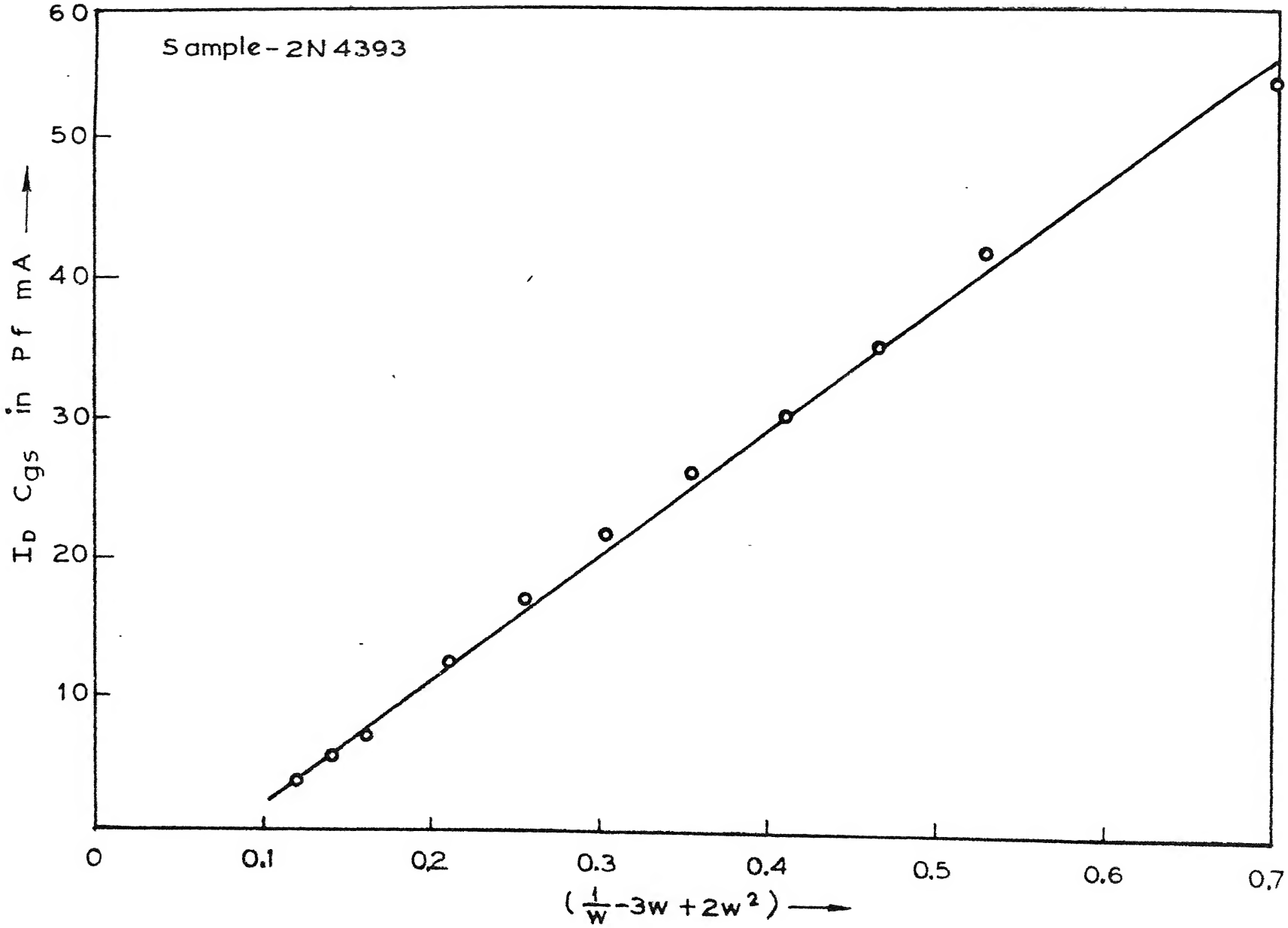


FIGURE - 5.8(a) PLOT OF I_D C_{gs} Vs. $(\frac{1}{W} - 3W + 2W^2)$

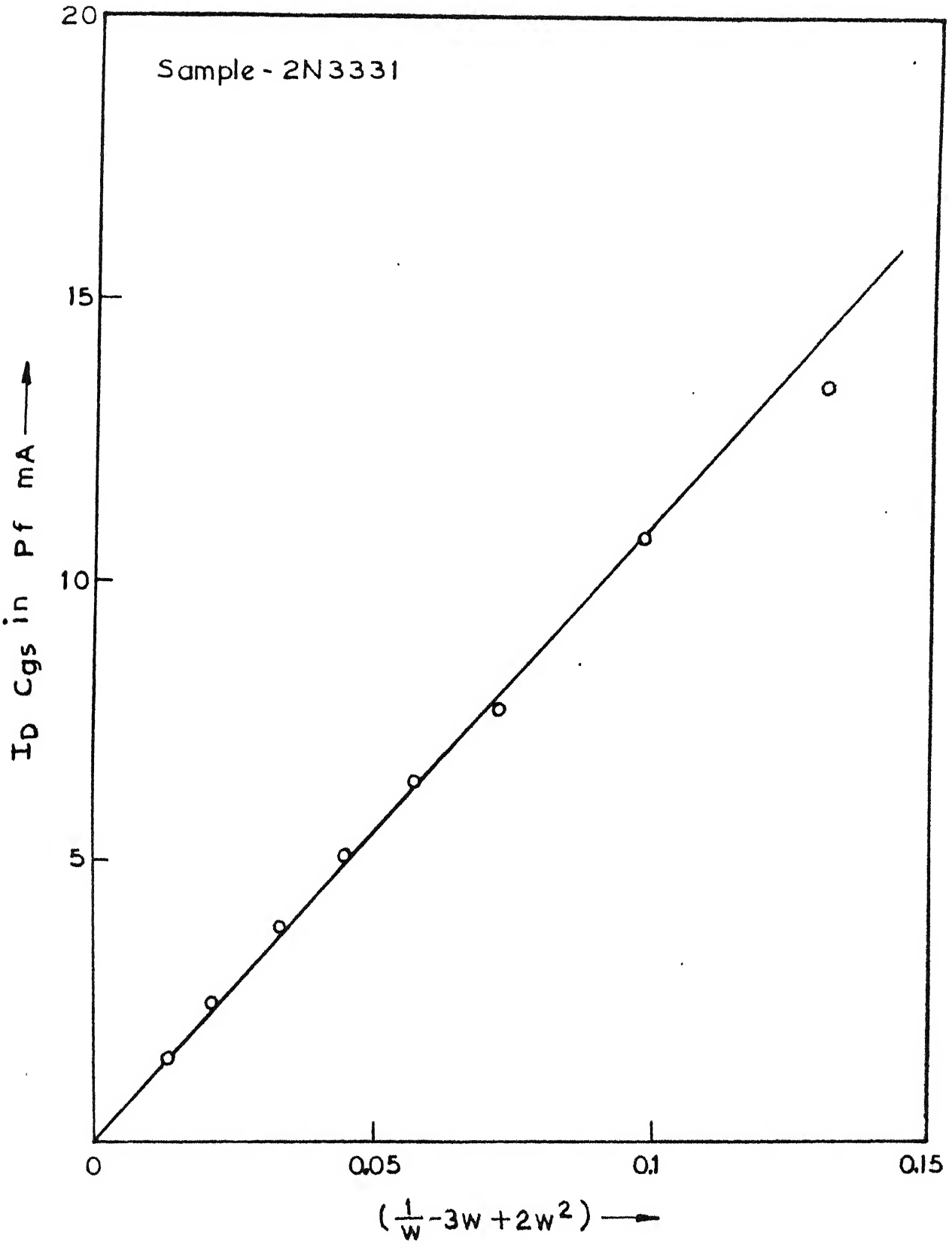


FIGURE - 5.8(b) PLOT OF I_D C_{gs} Vs. $(\frac{1}{W} - 3w + 2w^2)$

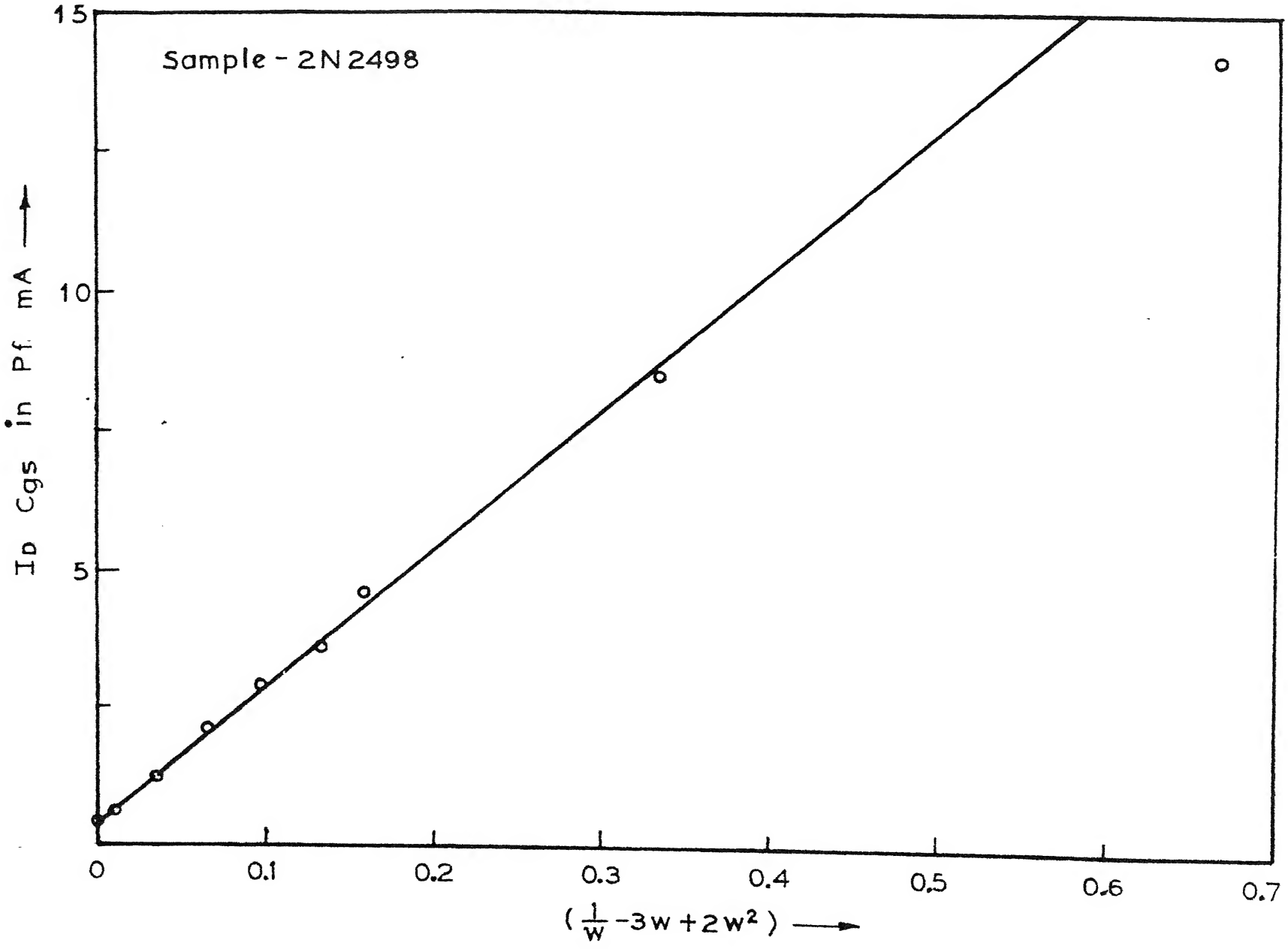


FIGURE - 5.8(C) PLOT OF I_D Cgs Vs. $(\frac{1}{W} - 3W + 2W^2)$

An examination of the values presented in table 5.8 shows that the discrepancy between the calculated and experimental values of the device parameter combination $\frac{L^2 g_o^2}{12 \mu_o}$ is wide. However, the agreement within the order of magnitude is obtained for each of the samples. The cause behind this discrepancy is likely to be accountable to the fact that the measurement of c_{gs} has been done under continuous d-c bias in the post-pinchoff condition. So, the amount of power dissipation within the device would have raised the temperature to a value higher than that of the ambient. Hence the value of the current I_D and the value of c_{gs} have suffered an appreciable change. It may be recalled that c_{gs} has not been considered as a circuit parameter for the determination of the device parameters in section 5.2.

In the next chapter a few suggestions about the improvement of the present method together with the concluding remark are presented.

REFERENCES

1. Caughey, D. M. and Thomas, R. E. - 'Carrier Mobilities in Silicon Empirically Related to Doping and Field' - IEEE Proceedings, Vol. 55, 2192, 1967.

2. Canali, C., Ottaviani, G. and Alberigi Quaranta, A. 'Drift velocity of Electrons and Holes and Associated Anisotropic Effects in Silicon' - Journal of Physics and Chemistry of Solids, Vol. 32, pp 1707, 1971.

CHAPTER - VI

CONCLUSION

A method has been outlined for determination of the geometrical and material parameters of JFET from the measured values of four circuit parameters. Behaviours of the JFET under (i) parallel-channel, (ii) gradual-channel and (iii) post-pinchoff models of operation have been studied to obtain a set of reliable relationships between the device and the circuit parameters. The parallel-channel model which applies equally well both for long- and short-channel JFETs has been found to yield three such relationships :

(i) the open channel conductance g_o,

(ii) the pinchoff voltage V_p, and

(iii) the reverse-bias gate-channel capacitance c_g.

It has been observed that the gradual-channel model is not capable of furnishing any additional information regarding device parameters. The fourth independent circuit parameter has been identified as the incremental drain-source conductance g_{ds} in the post-pinchoff operation.

The methodology is restricted at present only to long-channel JFETs due to the non-availability of any reliable model

for the pinch-off operation of short-channel silicon JFETs. It is, therefore, necessary to ensure that a given JFET is a long-channel device before the suggested method can be applied to determine the device parameters. A test for checking this criterion has been evolved on the basis of a property of the I_D-V_{DS} characteristics satisfied only by long-channel JFETs [1].

In the course of the study of existing parallel-channel models an inconsistency has been observed between the variations of c_g and g_o with V_{GS}. It has been shown that the inconsistency may be resolved by taking into account the effect of the floating substrate on the residual channel width. As a matter of fact, the substrate plays a very significant role in the modelling of the JFETs, not only in the parallel-channel regions of operation but also in other regions of operation. Indeed, it appears that the neglect of the effect of the substrate in the gradual-channel model is responsible for the discrepancy between the values of $\frac{zL}{a}$ obtained from the determined values of z,L,a and that given from the measurement of c_{iss}.

The experimental measurements carried out in the course of the present work exploit some conventional methods as well as some novel techniques. Those novel techniques are summarised below.

(i) Measurement of the conductance g_o of a totally pinched-off channel by forward biasing the gate-channel junction

has been developed and the pinchoff voltage V_p and the built-in voltage V_{bi} across the gate-channel junction for a complete depletion of the channel have also been found. The extent of forward biasing has been checked by monitoring the flow of gate current and the channel conductance has been measured from the two juxtaposed plots as shown in Figure 2.3(a). The pinchoff voltage V_p and the built-in voltage V_{bi} are obtained as the magnitudes of the gate-source voltage for complete cutoff and complete conduction condition of the channel respectively.

(ii) A scheme for measurement of g_{ds} with a pulsed bias has been developed where the device power dissipation is limited to a very low value. A small signal a-c voltage is added with the pulsed bias and the measurements of the bias voltage, bias current and g_{ds} are carried out with nulling techniques where the oscilloscope is used to serve the purpose of a detector.

The applicability of the present methodology is restricted only to long-channel JFETs. In order that a similar process be developed for short-channel JFETs also one can think of two possible alternatives - (a) the development of a reliable post-pinchoff model for short-channel JFETs, and (b) the extraction of one more information from the parallel-channel model itself. While the difficulty in the first approach has already been pointed out [2], the second alternative has not been fully explored. One feature of the open channel conductance, viz. the

variation of g_o with temperature appears to have a strong potential in this direction. As evident from the plots of Figure 2.3(b), the location of the peak in g_o vs T plot is characteristic of each device and it is the author's conjecture that the temperature at which g_o is maximum is a function of channel impurity concentration alone, independent of the device geometry. This information can be utilised if the theoretical basis for the peak in g_o vs T plot is analytically or empirically established in terms of the device parameters.

The device parameters, obtained from circuit measurements are the effective parameters and may be employed to obtain any circuit parameter at any applied bias and temperature. One very important utilisation of these effective device parameters would be in computer-aided design of electronic circuits, where the performance of the circuit containing JFETs need be optimised.

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1. Wedlock, B.D. - 'On Field Effect Transistor Characteristics', IEEE Transactions, Vol. ED-15, pp.181, 1968.

2. Chiu, T.L. and Ghosh, H.N. - 'Characteristics of JFET with Short Channel Length', Solid State Electronics, Vol. 14, pp. 1307, 1971.

APPENDIX - A.1.

DERIVATION OF COMMON SOURCE INPUT CAPACITANCE

a) Constant mobility

As shown in Chapter 3, c_{iss} may be obtained as

$$c_{iss} = \frac{\varepsilon z}{a} \int_o^L \frac{dx}{y(x)} \qquad .. \quad (A - 1.1)$$

where $y(x)$ is the depletion layer height normalised with respect to the undepleted channel height a.

For constant mobility, drain current I_D may be expressed according to Bockemuehl as

$$I_D \, dx = z\mu_o \, (N_o q)^2 \, a^2 y \, (1-y) \, dy \qquad .. \quad (A - 1.2)$$

or $$\frac{dx}{y(x)} = \frac{z\mu_o \, (N_o qa)^2 \, (1-y) \, dy}{I_D} \qquad .. \quad (A - 1.3)$$

Substituting in the expression for c_{iss} one obtains

$$c_{iss} = \frac{\varepsilon z}{a I_D} \int_{x=o}^{x=L} z\mu_o \, (N_o qa)^2 \, (1-y) \, dy \qquad .. \quad (A - 1.4)$$

I_D may be expressed as

$$I_D = \frac{1}{L} \int_o^L I_D \, dx$$

or $$I_D = \frac{1}{L} \int_{x=o}^{x=L} z\mu_o \, (N_o qa)^2 \, y(1-y) \, dy \qquad .. \quad (A - 1.5)$$

Substituting the value of I_D in equation (A - 1.4) one

obtains

$$\frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \frac{\int_{x=0}^{x=L} y\,(1-y)\,dy}{\int_{x=0}^{x=L} (1-y)\,dy} \qquad .. \quad (A - 1.6)$$

Let $y = 1 - u$, $y\big|_{x=0} = 1 - u_1$ and $y\big|_{x=L} = 1 - u_2$

u_1 and u_2 are the normalised residual channel heights at the source and drain end respectively. Then one obtains

$$\frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \frac{\int_{x=0}^{x=L} u(1-u)\,du}{\int_{x=0}^{x=L} u\,du} \qquad .. \quad (A - 1.7)$$

or $$\frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \left[1 - \frac{\int_{x=0}^{x=L} u^2\,du}{\int_{x=0}^{x=L} u\,du} \right] \qquad .. \quad (A - 1.8)$$

$$= \frac{a}{\varepsilon z L} \left[1 - \frac{2}{3} \frac{u_1^3 - u_2^3}{u_1^2 - u_2^2} \right] \qquad .. \quad (A - 1.9)$$

$$u_1 = 1 - \sqrt{\frac{-V_{GS} + V_{bi}}{V_p + V_{bi}}}$$

and $u_2 = 1 - \sqrt{\frac{-V_{GD} + V_{bi}}{V_p + V_{bi}}}$ are the residual channel heights at the source and drain ends respectively.

b) Field dependent mobility

For field dependent mobility the drain current I_D may be expressed according to Dacey and Ross as

$$I_D^2 dx = 2\sigma_o^2 E_c a^2 u^2 z\,(1-u)\,du \qquad .. \quad (A - 1.10)$$

where $\sigma_o = N_o q \mu_o$ is the low field conductivity

E_c = Critical electric field for the square root dependent mobility given by,

$$\mu = \mu_o \sqrt{\frac{E_c}{E}} \qquad .. \quad (A - 1.11)$$

where μ is the high field mobility at the field E and u is the **residual** channel height normalised with respect to 'a'. Substituting equation (A - 1.11) in (A - 1.1) one obtains

$$c_{iss} = \frac{\varepsilon z}{a\, I_D^2} \int_{x=o}^{x=L} 2V_p\, \sigma_o^2\, E_c z a^2\, u^2\, du \quad .. \quad (A\text{-}1.12)$$

Replacing I_D^2 as

$$I_D^2 = \frac{1}{L} \int_o^L I_D^2\, dx$$

one obtains

$$c_{iss} = \frac{\varepsilon z L}{a} \frac{\int_{x=o}^{x=L} u^2\, du}{\int_{x=o}^{x=L} u^2 (1-u) du} \qquad .. \quad (A - 1.13)$$

$$\text{Now} \quad \frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \frac{\int_{x=o}^{x=L} u^2 (1-u)\, du}{\int_{x=o}^{x=L} u^2\, du} \qquad .. \quad (A - 1.14)$$

$$\text{or} \quad \frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \left[1 - \frac{\int_{x=o}^{x=L} u^3\, du}{\int_{x=o}^{x=L} u^2\, du} \right] \qquad .. \quad (A - 1.15)$$

$$\text{or} \quad \frac{1}{c_{iss}} = \frac{a}{\varepsilon z L} \left[1 - \frac{3}{4} \frac{u_1^4 - u_2^4}{u_1^3 - u_2^3} \right] \qquad .. \quad (A - 1.16)$$

where u_1 and u_2 have been defined earlier.